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Two-Phase Drive Self-Scanning Light Emitting Device (SLED) Using Coupling Diodes

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The self-scanning light emitting device (SLED) is expected to become a new key device for two-dimensional optical information processing. Because the light emitting ON-states of SLED are automatically transferred by input clock pulses, and the optical pulses can start the transfer action from any elements. It is important to decrease the number of transfer clock lines for realizing the highly packed two-dimensional integrated SLED. So, we propose the two-phase drive SLED using coupling diodes, and demonstrate its operation. It has a wide operating margin and also has 10MHz as the maximum transfer frequency.

1.INTRODUCTION

Recently the research of opto-electronic switches using light emitting thyristors with pnpn-structure are actively undertaken. Most of these researches are intended to apply to photonic switching[1] for optical data transmission, and to memory cells[2-4] and optical comparators[5] for optical information processing.

We proposed a new functional opto-electronic device, "self-scanning light emitting device (SLED)".[6] The SLED consists of integrated light emitting thyristors whose light emitting ON-states are automatically transferred by input clock pulses, and optical pulses can start the transfer action from any elements. Therefore the SLED is expected to become a new key device for optical information processing with two-dimensionally integrated elements. Previously, We reported the resistor coupled SLED,[6] which needs three clock lines. However, it is important to decrease the number of transfer clock lines for realizing the highly packed two-dimensional integrated SLED. In this paper, we present a two-phase clock drive SLED using coupling diodes instead of resistors.

2.OPERATION PRINCIPLE

Figure 1 shows the equivalent circuit of the two-phase clock drive SLED using coupling diodes, which consists of light emitting thyristors with pnpn structure (T(-1)-T(3)), two transfer clock lines ϕ_1 and ϕ_2, coupling diodes D and gate resistors R_G. V_{GA} (=-5V) is the bias voltage.

The cathode turn-on voltage is nearly equal to V_G-V_{dif}, where V_G is the gate

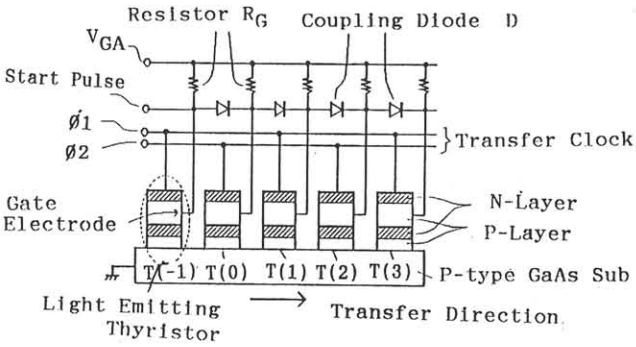

Fig.1 Equivalent circuit of two-phase drive SLED

potential and V_{dif} is the diffusion potential. When the thyristor T(0) is at ON-state with the low level of the clock $\emptyset_2$, the gate potential is nearly equal to the anode potential and T(0) emits light. The gate potential distribution, as shown in Fig.2, is formed by the gate current of T(0) through the coupling diodes. The next low level voltage of clock pulse $\emptyset_1$ after $\emptyset_2$ is applied to the cathodes of T(-1), T(1) and T(3), simultaneously. The appropriate low voltage of $\emptyset_1$ can turn-on only T(3) utilizing the differences of the gate potential between T(-1), T(1) and T(3). Therefore, the ON-state can be transferred to the right hand side by the two-phase transfer clock pulse.

To start the transfer action, an electrical or an optical start pulse is needed beside the transfer clock pulses. The electrical start pulse makes the start element turn-on by pulling up the gate potential from -5V to 0V with the low level of the clock $\emptyset_1$.

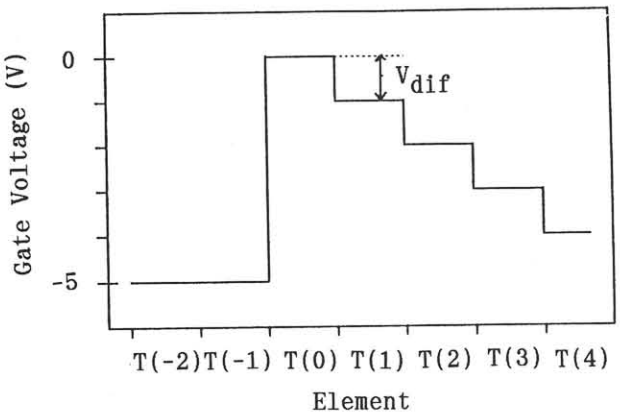

Fig.2 Gate potential distribution

3.FABRICATION AND DEMONSTRATION

3.1 Fabrication

To demonstrate the two-phase drive SLED using coupling diodes, 12bits and 62.5μm pitch thyristor arrays, coupling diodes, and gate resistors are fabricated monolithically on p-type GaAs substrate. The diode coupled SLED can be fabricated in the same process as the resistor coupled SLED,[7] because the coupling diode can be formed using the top n-layer, as shown in Fig.3. R_p denotes the parasitic resistance in the gate p-layer. The pnpn-GaAs epitaxial films, which has double hetero-structure for carrier confinement and high external quantum efficiency, were grown on the p-type GaAs substrate by the MOVPE method. The film thicknesses and carrier densities of each layer are listed in Table 1.

The process flow of the SLED is shown in Fig.4. The fabrication process consists of 8 photolithographic steps. By the 1st photolithographic step, the insulating SiO_2 film was deposited on the epitaxial films and formed by etching. The AuGeNi alloy on the top n-layer was formed by lift-off process (2nd photolithographic step). Next

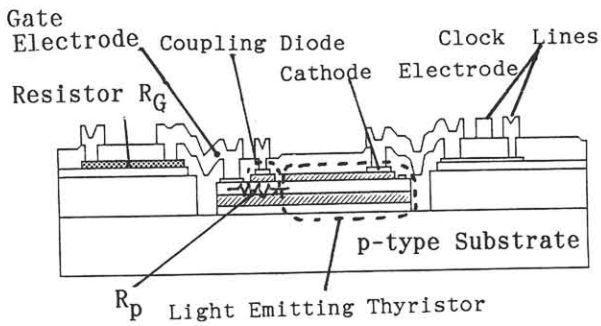

Fig.3 Cross-section of the SLED

Table 1 Film thicknesses and carrier densities

layer	thickness	carrier density (cm^{-3})
6th n-GaAs	150nm	$2X10^{18}$
5th n-$Al_{0.3}Ga_{0.7}As$	400nm	$3X10^{18}$
4th p-GaAs	1.0μm	$1X10^{17}$
3rd n-GaAs	300nm	$1X10^{18}$
2nd p-$Al_{0.3}Ga_{0.7}As$	420nm	$1X10^{18}$
1st p-GaAs	500nm	$2X10^{18}$
p-substrate	450μm	$1X10^{19}$

the top n-layers was etched away by the 3rd step. The Cr-SiO cermet was deposited by electric beam evaporation as the resistors. And the AuZn alloy was deposited as the gate electrodes. They were patterned by lift-off processes (4th and 5th steps). And then, each thyristor was isolated by etching the 3rd n-layer and 4th p-layer away (6th step). The insulating polyimide film was coated and the through holes were opened by the reactive ion etching (RIE) using O_2 and CF_4 gases (7th step). The Al film was deposited on the polyimide film and etched away by the last photolithographic step. Finally, the AuZn alloy was deposited on the back of the substrate and annealed for making ohmic contact.

Figure 5 shows the photomicrograph of fabricated SLED chip, which consists of 12 bits thyristor array, coupling diodes, transfer clock lines and the gate resistors. We obtained 30kΩ as R_G.

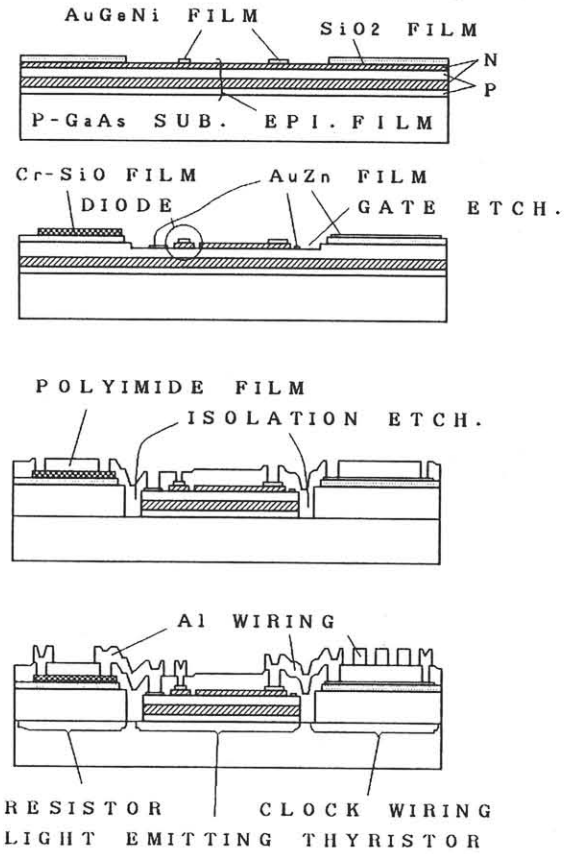

Fig.4 Process flow of the SLED

3.2 Demonstration of self-scanning operation

The self-scanning operation of two-phase drive SLED is observed within the wide range of the low level voltage of clock pulses from -4V to -9V, when the bias voltage V_{GA} is -5V and high level voltage of clock pulses is 0V. This operating margin of the diode coupled SLED, about 5V, is larger than the resistor coupled SLED whose margin is 2V.[7] The obtained maximum transfer frequency is 10MHz. The CCD image of the transferring SLED is shown in Fig.6, and the gate voltage waveform of the 12th element, T(12), is shown in Fig.7.

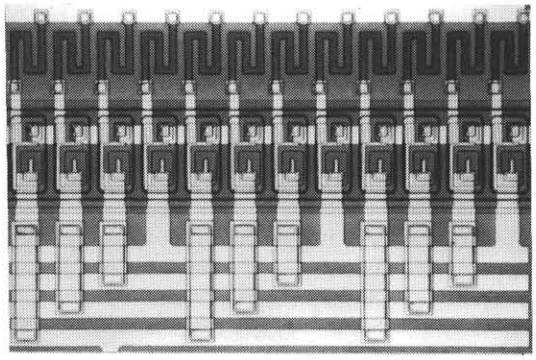

Fig.5 Photomicrograph of fabricated SLED (The photomicrograph shows the four-phase drive SLED. We observed the two-phase drive operation by connecting $\emptyset_1$ with $\emptyset_3$ and $\emptyset_2$ with $\emptyset_4$, respectively.)

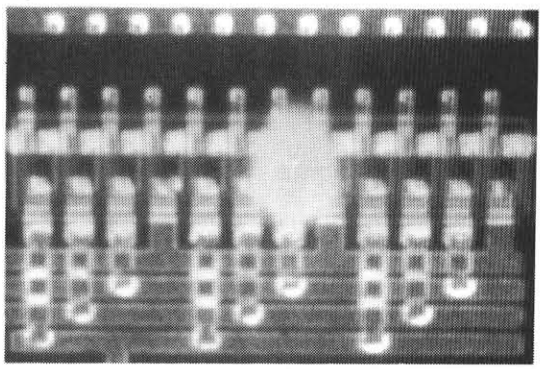

Fig.6 The CCD image of the transferring SLED

3.3 Effect of the parasitic resistance of gate layer

The gate potential distribution suggested by Fig.7 shows that the ON-state element affects the gate potential of only two elements of its right hand side, and it is different from Fig.2.

The potential difference is due to the voltage drop by the high internal parasitic resistance R_p ($\sim$100kΩ) between the gate electrode and the coupling diode. The equivalent circuit including the parasitic resistance is illustrated in Fig.8, when the element T(0) is at ON-state, where R_{p-1}, R_{p1} and R_{p2} shows the parasitic resistance. The parasitic resistance of T(0) is neglected because of the conducting modulation accompanied by the ON-state. Therefore, the gate potential of T(1) is about $-V_{dif}$. The potential difference caused by the resistor R_{p1} pulls the gate potential of T(2) down. Moreover, the gate potential of T(3) is pulled down to almost V_{GA}.

The parasitic resistances are useful for wide operating margin. Because the ON-state of the element T(0) is transferred by utilizing the difference of the gate potential between T(1) and T(3), which corresponds to operating margin. It has disadvantages, however, the parasitic resistances give rise to the turn-on voltage shift and ununiformities.

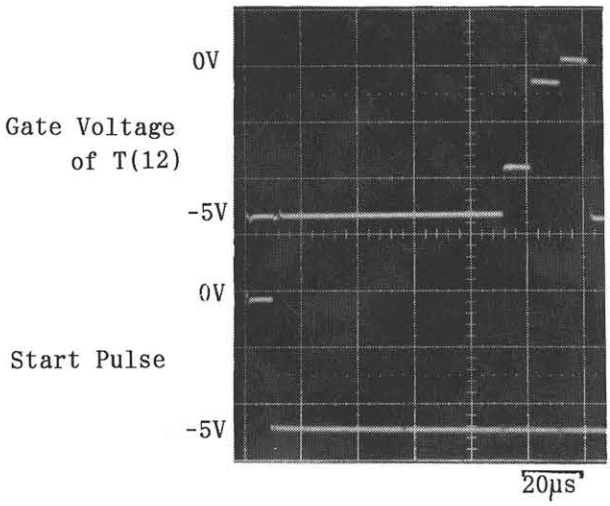

Fig.7 Gate voltage waveform of the 12th element(transfer frequency is 100kHz)

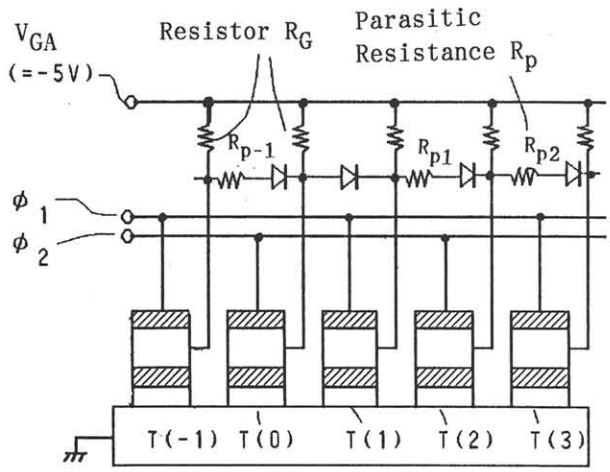

Fig.8 Equivalent circuit of SLED concluding the parasitic resistances

4.CONCLUSION

The two-phase clock drive, diode coupled SLED is proposed and demonstrated. It has a wide operating margin and also has 10MHz as the maximum transfer frequency. The diode coupled SLED will be useful for realizing the highly packed two-dimensional OEIC for optical information processing.

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