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Design of Optically Coupled Three-Dimensional Content Addressable Memory

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An optically coupled three-dimensional content addressable memory is newly proposed for parallel data processing. Several memory layers are stacked in this memory. The memory cell consists of three parts for data store, data matching and data transfer. The optically coupling flip-flop with LEDs and photoconductors is employed in the data transfer part. Simultaneous data inspection through several memory layers can be implemented by optical coupling. Consequently, the inspection speed and the memory address space is significantly increased.

1. Introduction

It is known that the performance of the bus connection type parallel processing computer system with multi-processors is limited by the data communication efficiency of the signal bus because it is difficult to implement the parallel data transfer among the processors and the memories. To overcome this problem, we have hitherto proposed a new method for parallel processing where a new optically coupled three-dimensional common memory (3D-OCC memory) is used instead of the conventional signal bus¹⁾. This 3D-OCC memory, which is considered as a multi-bus with memory function, has a new function of simultaneously implementing the parallel data transfer and the data latch for a block of data. A large block of data can be simultaneously transferred with very high speed by optical coupling in the vertical direction, while the conventional memory operations are carried out in the horizontal memory planes. It has been revealed that the ultra fast data transfer speed of 128Gbit/s can be achieved by using 3D-OCC memory^{2,3)}. In this paper, we further propose a new optically coupled three-dimensional content addressable memory (3D-OCAM) which can realize the real time parallel processing computer system by combining with such 3D-OCC memory and dramatically increase the memory address space by employing three-dimensional virtual memory function.

2. Concept of 3D-OCAM

Figure 1 depicts an example of a real time parallel processing computer system with the 3D-OCAM and the 3D-OCC memory. In this system the virtual memory function can be simultaneously applicable for all local memories by using the 3D-OCAM. A memory layer is optically coupled with the upper and lower memory layers both in the 3D-OCAM



with three-dimensional optically coupled memory.

and 3D-OCC memory. Therefore, data written into a memory layer are simultaneously transferred to other memory layers to share them among all memory layers. The virtual memory function can be implemented by optically transferring the logical address data given to the 3D-OCAM, and then executing the read/write operation to the local memories after transforming the logical address data to the physical address data. Usable memory space is dramatically increased in this virtual memory system since one CPU can use the very large virtual memory space which consists of all local memories but not only the corresponding local memory. This large virtual memory space is shared among all CPUs. The 3D-OCC memory in Fig. 1 is used for simultaneously executing many instructions in parallel, sharing the data read-out from the local memories by 3D-OCAM among all CPUs.

Figure 2 shows the memory cell circuit for the 3D-OCAM. The memory cell consists of three parts for data store, data matching and data transfer. The optically coupling flip-flop is employed in the data transfer part. The data are transferred in the vertical direction by optical coupling, storing the data into the optically coupling flip-flop. In the matching part, the data in the data store part are compared with both inspection data stored in the data transfer part for the vertical inspection through all memory layers and those given to the bit lines from the data lines for the horizontal inspection inside a memory layer. Both vertical and horizontal inspections are simultaneously implemented.

3. Optically Coupling Flip-Flop

The optically coupling flip-flop consists of the data store flip-flop and the LED drive circuit as shown in Fig. 3. The data store flip-flop is composed of MOS transistors Tr1 and Tr2, and photoconductors PC1 and PC2. The LED drive circuit is composed of MOS transistors Tr5, Tr6 and Tr7, and LED1 and LED2. One of two LEDs emits the light, corresponding to the data stored in the data store flipflop, to optically transfer the data to other memory layers by driving the LED control line after writing the data into the data store flip-flop. When the signal light transferred impinges onto either of two photoconductors, the resistance of the lightilluminated photoconductor is decreased and con-



Fig. 2 Memory cell and peripheral circuits of 3D-OCAM.





sequently the node voltage levels of the data store flip-flop are inverted. Thus, the transferred data are directly written into the data store flip-flop without passing through the access transistors Tr3 and Tr4.

The optical data transfer speed in the optically coupling flip-flop strongly depends on the optical coupling efficiency between the LED and photoconductor. The optical coupling efficiency as large as possible should be used in order to increase the data inspection speed by increasing the optical data transfer speed. It is noted that the light emitted from an LED impinges not only onto the corresponding photoconductor as a signal light but also onto the adjacent photoconductors as stray lights. Therefore, it is required to increase the optical coupling efficiency for the signal light, decreasing that for the stray lights. Then, we evaluate the influences of the optical coupling efficiency for the signal light and stray lights on the optical data transfer time. The data transfer time is plotted versus the optical coupling efficiency for the signal light in Fig. 4. The LED size and the photoconductor size are $5 \times 5 \mu m^2$ and $10 \times 10 \mu m^2$, respectively. The vertical spacing between the LED and photoconductor is 5μ m. These device parameters give rise to the optical coupling efficiency of 1.4% for the signal light. Therefore, it is obvious from Fig. 4 that the LED current should be 275μ A or more in order to reduce the optical data transfer time to less than 10ns. Figure 5 shows the dependence of the data transfer time on the optical coupling efficiency for the stray light. As is clear from the figure, the data transfer time is significantly increased with increasing the optical coupling efficiency for the stray light. However, the optical coupling efficiency can be reduced to less than 0.01% by increasing the device pitch to larger than 20 μ m. Thus, the data transfer time shorter than 10ns can be achieved even after the stray light effect is taken into account.

4. Data Matching Circuit

The inspection operation in the data matching circuit is implemented by comparing the data in the data store part with those in the data transfer part and those given to the bit lines. The match line is pre-charged to the high voltage level before matching operation. This high voltage level is discharged to the GND level through the transistors





M1, M3 and M5 or M2, M4 and M6 when the data are not matched in the vertical inspection. When the data are matched, the voltage level of the match line remains the high level. The optical match line is used for detecting the matched data in the vertical inspection operation among many memory layers, while the electrical match line is used for the horizontal inspection operation within an identical memory layer.

5. Parallel Inspection through Multi-Layers

Figure 6 indicates the waveforms for the parallel data inspection operation with the 3D-OCAM which are obtained by performing the optical-electrical circuit simulation⁴⁾. The inspection operation consists of three parts of electrical writing to the optically coupling flip-flop, the optical data transfer to other memory layers, and simultaneous data matching between the data store flip-flop and the optically coupling flip-flop. As is obvious in the figure, the inspection data are written into the optically coupling flip-flop through the bit lines (BLs). The node voltage levels of the flipflop are inverted by applying the pulse to the optical word line (OWL) after pre-charging bit lines and turning-on the transfer gate (TG) after giving the inspection data to the data lines (DL). Then, the inspection data are sequentially transferred to other memory layers by driving the LED control line (LCL). The data transfer time from the first layer through the second and third layers to the fourth layer is 36ns. The matching operation is simultaneously implemented in all memory layers by driving the matching control line (MCL) after the inspection data are written into the optically coupling flip-flop in all memory layers. It is obvious from Fig. 6 that one inspection operation through four memory layers can be achieved within a very short time of 90ns which is equivalent to the data inspection time of 22.5ns per one layer in spite of $2\mu m$ CMOS design rule used. Thus, it is confirmed that the high speed data inspections through many memory layers and the virtual memory operation can be realized by using the 3D-OCAM.



Fig. 6 Wave forms for the multilayerinspection operation of 3D-OCAM.

6. Summary

We have proposed a new optically coupled threedimensional content addressable memory (3D-OCAM) which dramatically increases the virtual memory space in the real time parallel processing computer system. It has been revealed that the very high speed data inspection of 22.5ns per one memory layer can be achieved even if $2\mu m$ CMOS design rule is used.

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