Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 769-772

S-B-3

Fabrication of Vertical Cavity Front Surface Emitting Laser Diode (FSELD) Using HBT Process

Hoi-Jun Yoo, J. R. Hayes, N. Andreadakis, E. G. Paek, J. P. Harbison, L. T. Florez
and
Young-Se Kwon*

BELLCORE, RedBank, NJ 07701-7040, USA.
*Dept. of E.E., KAIST, Cheongryang P.O. Box 150, Seoul, Korea.

We have investigated a front surface emitting laser diode (FSELD) and a Top Electrode FSELD which emit laser light from the front surface of the wafer. Since their structure is similar to that of HBT, they were fabricated using the conventional HBT process and mask sets. The current flows bypassing the high series resistance DBR stacks and active layer is surrounded by an oxygen implanted semi-insulating layer. They showed a low series resistance and small threshold current, 6mA for 25μm diameter laser.

I. Introduction

Surface emitting lasers are of interest for various applications[1-3], (eg. parallel signal processing, high speed optical interconnects and two-dimensional phase-locked arrays) because it can be fabricated using a monolithic process without wafer cleaving for the mirror formation. More specifically, vertical cavity surface emitting laser diodes(VC-SELD) offer potentially a higher packing density, larger emitting areas, better beam quality, unconstrained arrangement of emitters.[1] Most of all, it can be fabricated using a fully planar technology with easy batch processing and complete compatibility with fabrication process of conventional electronic devices. However, there has been no report on the vertical cavity surface emitting laser diode (VC-SELD) of which fabrication process is compatible with that of conventional electronic devices.

The VC-SELD has a clear disadvantage of a small volume of optical gain region which impedes the progress of VC-SELD study. Therefore, one should confine the optical field and electrons tightly into the active region to increase the interaction between photons and electrons reducing the optical loss. Recently, there have been several reports of low threshold current operation using VC-SELD's comprising high reflectance mirrors and tight current confinement to reduce the threshold current.[4,5] However, the semiconductor stacked layers forming the high reflectance mirror caused the problem of a large series resistance leading to higher power consumption above threshold, in spite of the low laser threshold current. Also, the large step height of the mesa forming the laser makes it difficult to integrate this device with other electronic and/or optoelectronic devices. In addition, its active layer is exposed to air having a leakage current problem due to surface recombination current.

In this paper we investigated front surface emitting laser diodes (FSELD's) which are suitable for the batch processing compatible with conventional planar technology. That is, its fabrication process is similar to that of high speed heterojunction bipoalar transistor (HBT)[6] and therefore, they can be easily incorporated into optoelectronic integrated circuits (OEIC).

II. Laser Structure

Front Surface Emitting Laser Diode (FSELD) has a clear difference from the conventional

VC-SELD in that it has a relatively planar structure. Fig. 1 and 2 illustrate the schematic diagrams of FSELD's. Fig. 1 has the n-electrode on the bottom surface and Fig. 2 has both the p and n electrodes on the top surface. They have a strained Q.W. active layer surrounded by semi-insulating layer prepared by a double ion implantation technique. The advantages of these FSELD's include the following points. 1) The laser light emerges from the front surface of the wafer and therefore,both the electrical and optical input/output terminals can be accessed on the front surface. In addition, the limitation in emission wavelength which comes from the substrate absorption is removed making this structure attractive for the fabrication of various emission wavelength SELD, such as a visible laser. 2) Since it has a planar surface and its fabrication process is exactly same as that of high speed HBT's, optoelectronic integrated circuits incorporating FSELD can be easy to realize and have the potential for large scale integration. 3) FSELD does not use the top DBR as a carrier injector any more, but pure optical mirror. Therefore, semiconductor stacks are not necessary always and other material systems like dielectrics or metals can be used to optimize the mirror reflectance and reduce the total step height of the device. Moreover, the integration of thin film photonic devices on the FSELD is rather easily obtained by stacking them. 4) Usually the high series resistance of VC-SELD comes from p-type DBR, but FSELD flows current bypassing it reducing the series resistance and power consumption of the device. 5) Its active layer is surrounded by a semi-insulating layer and there is no leakage current from the surface recombination leading to a low threshold current. These advantages will provide a new possibility of three dimensional optoelectronic integrated circuits (3D-OEIC) to current OEIC technology.

III. Fabrication

A schematic diagram outlining the fabrication process of the FSELD is shown in Fig. 3. The FSELD comprised an AlAs/GaAs bottom DBR layers, an AlGaAs lower cavity layer, an InGaAs

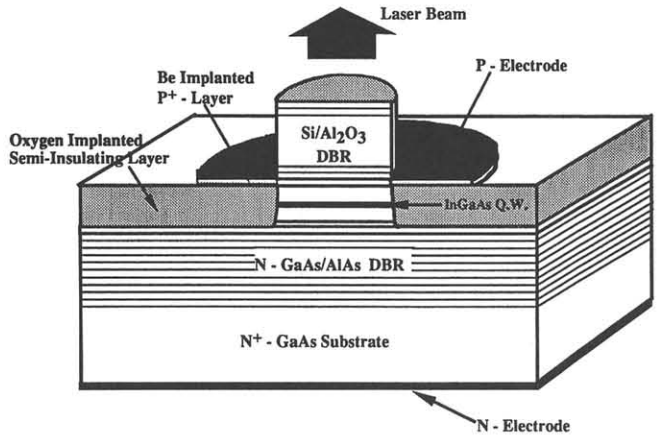

Fig. 1 Schematic diagram of a Front Surface Emitting Laser Diode (FSELD).

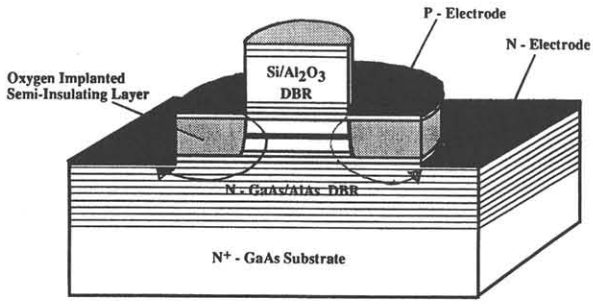

Fig. 2 Schematic diagram of a Top Electrode Front Surface Emitting Laser Diode.

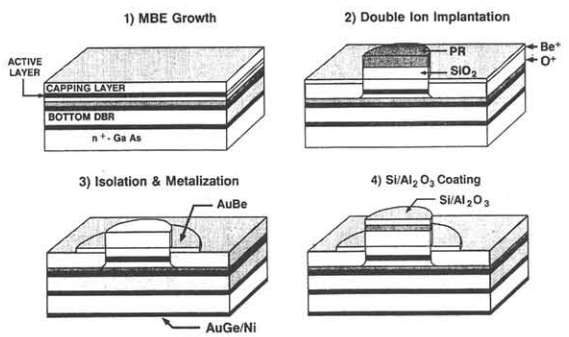

Fig. 3 Schematic diagram illustrating the fabrication process of a FSELD.

strained quantum well active layer, an AlGaAs capping layer and an AlAs/GaAs top DBR layers grown on a n^+-GaAs substrate by molecular beam epitaxy. Actually, the top DBR is not essential for the fabrication of the FSELD since we intend to use a Si/Al_2O_3 dielectric stacks for the top mirror but was included for the subsequent fabrication of a mesa etched surface emitting laser for the purpose of comparison. A part of the wafer was processed to make mesa etched surface emitting laser. The

remaining section of the wafer had the top mirror removed by ion-beam milling and wet chemical etching to a point close to the AlGaAs capping layer. Therefore, only the bottom DBR remains, in contrast to a conventional InGaAs active layer surface emitting laser. Since the current flows through only one DBR mirror and in the also the electron injector, a low series resistace diode can be obtained.

To fabricate the FSELD thick SiO_2 layer was deposited on the etched surface using the PECVD method and etched to form 25μm diameter dots using HBT emitter mask. The photoresist and SiO_2 disc was then used as an ion-implantation mask for the O^+ implantation to form a high-resistivity layer around the active region. This prevents current leakage through the extrinsic active layer under the p-electrode and confines the injected current to the intrinsic active layer under the dielectric DBR. A subsequent Be^+ implantation was then carried out with the same mask in place to make a good ohmic contact to the extrinsic active region on the semi-insulating layer. Anealing was then performed of the sample, encapsulated in Si_3N_4 in a flow argon atmosphere for 20sec at 850 °C.

Following the anneal AuBe was evaporated onto the Be-implanted surface using standard electron beam evaporation and lift-off technique using HBT base metallization mask. The p-electrode was deposited around the SiO_2 dot that had a ring shape with an inner diameter of 25μm and an outer diameter of 65μm. After alloying, the remaining Be-implanted area was etched away using wet chemical etching to obtain device isolation. For the fabrication of Top Electrode FSELD, top of the n-DBR layers was exposed by a more etching. Then, with the standard lift-off technique, AuGe/Ni/Au layers were coated and alloyed for n-ohmic contact. The top DBR was made of an electron beam evaporated Si/Al_2O_3 stack on top of the SiO_2 and patterned using standard lift-off techniques. The

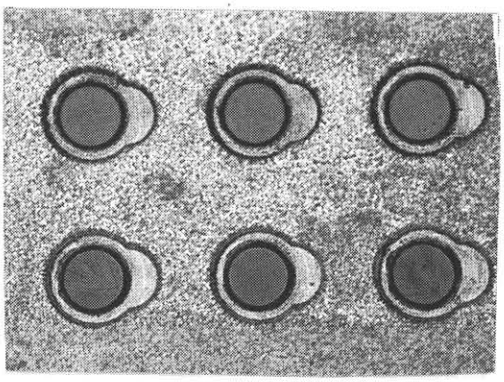

Fig. 4 Microphotograph of fabricated Top Electrode FSELD's.

backside of the wafer was lapped to ~100μm thickness and mirror polished with a 2% Br_2-MeOH solution. Since the light will emit from the front surface, a thick AuGe layer, ~0.5μm, was coated on the backside to enhance the thermal dissipation. A microscope photograph of a Top Electrode FSELD, fabricated using the double ion-implantation techniques described above, is shown in Fig.4.

IV. Results and Discussions

The forward current/voltage characteristics of the FSELD and mesa etched SELD of the same diameter are shown in Fig. 5. In addition, Fig. 6 shows the current/voltage characteristics of Top Electrode FSELD. As can be clearly seen in Fig. 5, the FSELD shows a current/voltage characteristics that has significantly less series resistance than the mesa etched SELD. For example, at an operating current of 4mA the FSELD has a voltage drop of 3V compared to 8V for the mesa etched SELD. As can be seen the addition of a good ohmic contact and one DBR leads to a significant reduction in the bias voltage at threshold. This may be true especially in p-type top DBR because the hole mobility is smaller than the electron mobility. This issue addresses more clearly in Fig. 6 because Top Electrode FSELD folws current bypassing both of the n and p DBR stacks. Its cut-in voltage is near 1V and series resistance is about 50Ω.

The lasing characteristics of FSELD's were evaluated at room temperature using 400nsec pulses operating at a 5KHz repetetion rate. FSELD and Top

Electrode FSELD had the same optical characteristics. Their measured light-current characteristics are shown in Fig. 7. A typical threshold current for a 25μm diameter FSELD is 6mA which is comparable to the lowest reported threshold current for any SELD. In comparison the mesa etched SELD, also having a 25μm diameter, fabricated from the same wafer shows a typical threshold current of 15mA. We think that the low threshold current of the FSELD is due to the tight current confinement in the active region resulting from the O^+-implanted semi-insulating region. In addition, if there is little, if any, surface recombination current because the active layer is surrounded by a semi-insulating material. The maximum light output is about 1mW and differential quantum efficiency is 0.25mW/mA. The spectrum of a typical FSELD above threshold is also shown in Fig.7. The lasing wavelength is 971nm and spectral linewidth, above threshold, is about 5 Å. For a range of currents up to several times the threshold current, only single mode operation is observed because the mode spacing is much large due to its short cavity length.

V. Conclusions

In conclusion, we have fabricated a front surface emitting laser diode (FSELD) and Top Electrode FSELD using a double ion implantation of oxygen and beryllium. The structures were found to have a low series resistance resulting from the low p-contact resistance and a low threshold current of 6mA resulting from both a tight confinement of current in the active region and minimal surface leakage. The 25μm diameter FSELD had a lasing wavelength of 971nm and a spectral line width of 5Å. Since there is no limitation in emission wavelength which comes from the substrate absorption, they can be used to fabricate various emission wavelength SELD, such as visible SELD.

1)K. Iga et al., IEEE J. Quantum. Electron., **QE-24**, 1845 (1988).
2)E. G. Paek et al., Proc. of SPIE 89, San Diego, CA.

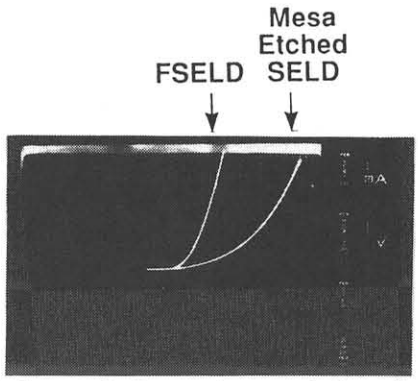

Fig. 5 Current/voltage characteristics of a FSELD and a mesa etched laser of the same diameter. (Ver. Scale = 1mA, Hor. Scale = 1V)

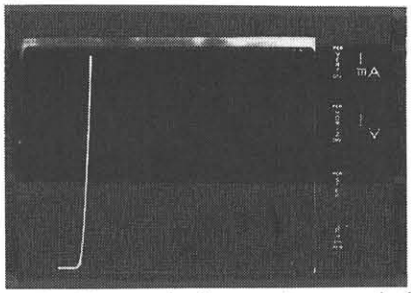

Fig. 6 Current/voltage characteristics of a Top Electrode FSELD of 25μm dia.(Ver. Scale = 1mA, Hor. Scale = 1V)

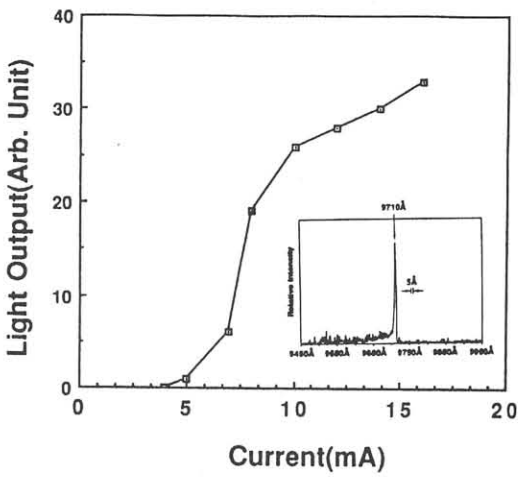

Fig. 7 Light output/current characteristics and optical spectrum above lasing threshold of a FSELD.

3)Hoi-Jun Yoo et al., IEEE J. Quantum Electron., June(1990).
4)A. Ibaraki et al., Japan. J. Appl. Phys., **28**, L667 (1989).
5)J. L. Jewell et al., Electron. Lett., **25**, 1123, (1989).
6)P. M. Asbeck et al., IEEE Electron. Dev. Lett., **EDL-5**, 310 (1984).