Invited

Work at STC Technology on InP-Based Integrated Optics and Integrated Optoelectronics for WDM Applications

G.H.B. Thompson

STC Technology Ltd

London Road, Harlow, Essex, CM17 9NA, UK.

New techniques for monolithic optoelectronic and optical integration on InP have been developed particularly for application in wavelength division multiplex optical transmission systems. A quasi planar process for the fabrication of InGaAs/InP receiver OEICs is reported, based on a single step MOVPE growth. A monolithic transimpedance receiver, incorporating a high gain cascode amplifier shows a sensitivity of -31.5 dBm at 1.2 Gbit/s for a BER of 10⁻⁹. Fully functional 4-channel transimpedance receiver arrays have been fabricated. An integrated grating demultiplexer operating in a slab-guided mode and utilising vertical dry-etched mirrors is described and the capabilities of the system discussed.

Introduction

High density wavelength division multiplex provides a means of increasing channel capacity in future optical systems in a way which can be introduced flexibly and does not require extremes of high bit rate. Its attractiveness would be further enhanced if the many parallel signal paths which occur at the multiplex and demultiplex stages could be integrated both optically and electronically on a single chip. Complexity, size and costs would be reduced and crosstalk more precisely controlled, which would be very worthwhile even if performance, in terms of speed or sensitivity, remained the same. Work at STC has been, so far, directed mainly to developing the multiple receivers and the demultiplexer needed in this system.

The primary aim at STC in the choice of an integration technology has been to obtain sufficient consistency in device performance and sufficient tolerance in the electronic circuitry to facilitate the practical production of adequately complex

OEIC's. Progress has been assisted by the adoption, where possible, of fabrication procedures closely related to the more mature GaAs IC technology, such as full wafer processing, planar structures, multilevel metallisation for interconnect, and elimination of multiple epitaxial growth steps. In this paper, we report significant achievements for both the numbers of integrated components on one receiver chip and for the performance of the individual receivers. We describe the first monolithically integrated four channel receiver array for 1.5 μ m wavelength operation comprising four separate transimpedance receivers, and containing a total of 88 components. Furthermore, measurements on a similar single channel receiver with somewhat smaller area pin diodes indicate a comparable sensitivity at 1.2 Gbit/s to commercially available hybrid pin/FET receivers.

For the wavelength demultiplexer a grating spectrometer offers the most convenient means of separating a large number of channels. As an alternative to conventional free space optics, we have investigated the use of slab waveguide techniques for making the spectrometer. These have the potential of making particularly small, robust and ultimately cheap optical components and when based on InP, are compatible with the integrated optoelectronics.

IC Fabrication Procedure

The IC technology is based on a quasi-planar process in which the relatively thick InGaAs layer for the pin diodes is grown by unmasked MOVPE in recesses in the semi-insulating InP substrate. 2" diameter wafers are used to improve processing quality and yield. In our normal process the layers for the InP/InGaAs heterojunctions FETs (HJFET) are grown beneath the pin layer during the same single stage of MOVPE, as is also the upper p⁺ InGaAs layer of the pin¹. Subsequent selective etching leaves the photodiodes sunk within the recesses, exposing the FET layers elsewhere. Figure 1 shows a schematic cross-section of the integrated devices. The wafer is planar except for a narrow moat around the detectors. In an alternative process no FET layers are grown and instead ion implantation is used to form InP JFETs directly in the substrate and photodiodes in the InGaAs layer². Conventional etching and metallisation steps are used to define the various device structures.



Figure 1. Schematic cross-section of photodiode integrated with HJFET.



Figure 2. Circuit diagram of receiver chip.

PECVD silicon nitride serves both as an anti-reflection coating and as a dielectric for MIM decoupling capacitors. Finally, polyimide is used to planarise the wafer surface and provide a low capacitance dielectric between the two levels of metal interconnection, as well as filling in the moat around the detectors. Resistors are formed from mesas of FET channel material, and the FET gate junction is used to make dc level shift diodes.

Receiver Performance

The circuit used for the monolithic receivers is a cascode transimpedance design as illustrated in Figure 2. The device parameters for the sensitive 1.2 Gbit/s receiver are as follows. The photodiode, with 20 µm window diameter has a responsitivity of about 0.95 A/W at λ = 1.3 μm and a capacitance of 60 fF, both measured at - 5V. The FETs have nominal gate lengths of 1.5 µm with 4.5 µm sourceto-drain spacing. The mean transconductance and drain conductance at Vg = 0 are about 60 and 3 mS/mm respectively. The FET gate capacitance at Vg = 0 is about 1 pF/mm plus about 35 fF parasitic associated mainly with the gate contact mesa. The mean feedback resistance is about 36 k Ω . The 3 dB

bandwidth of the transimpedance response is 700 MHz. The noise spectral characteristic corresponds to a sensitivity at 1.2 Gbit/s of -31.5 dBm for 10⁻⁹ BER. This is about 5 dB inferior to the best reported for (high impedance) hybrid pin/FETs⁴. The major part of the discrepancy can be attributed to excess channel noise in InGaAs FETs. The cause of this, which may be associated with avalanche multiplication, is at present being investigated.

The completed chip of a four channel transimpedance receiver is illustrated in Figure 3. This contains 36 FETs, 4 pin photodiodes, 24 level shifting diodes and 20 MIM capacitors. The receiver circuits are nominally the same as in the single channel receiver, except that the pin diodes have four times the window area. A number of receivers arrays have been tested and found to be fully operational⁵. The value of the feedback resistor is around 30 $k\Omega$ resulting in -3 dB bandwidths from 160 to 210 MHz for the four channels. Some crosstalk is observed between channels which varies from 0.5 to 5%. Its cause is under investigation.

Demultiplexer Design and Fabrication

The experimental demultiplexer' is illustrated schematically in Figure 4. It is based on a single-moded slab waveguide formed by the epitaxial growth by MOVPE of, in this instance, a single layer of GaInAsP on an InP substrate, although it would be desirable in an optimised device to cap this with an InP cladding layer. All optical operations are performed by the total internal reflection of the slabguided mode from semiconductor air interfaces. Such interfaces are produced by etching vertical-sided recesses through the epitaxial layer into the substrate. Light is input to the device by means of a single-moded ridge waveguide. The



Figure 3. 4-channel receiver array chip (3.7 x 3.2 mm).

diverging output from the guide is collimated by a parabolic mirror. After diffraction a similar mirror focuses the slab mode onto the end of an output waveguide. To avoid the need to reflectively coat the grating elements whilst maintaining high dispersion an unorthodox design of grating was used in this case. It operates in transmission and uses separate recesses as the individual elements. These are triangular in plan, so as to allow the diffracted beams unimpeded passage. Set at 45° in this particular case, and with collimating mirrors of about 600 μ m focal length, the grating gave a dispersion of about 1 μ m per nm wavelength interval at 1.5 µm. For a practical demultiplexer using, say, 3 μm source and image size and 4 nm channel



Figure 4. Integrated grating wavelength demultiplexer.

separation, higher dispersion would be needed, which would be most simply achieved by increasing the focal length.

The fabrication involves few stages. Both the mirrors and the waveguides are defined on an RF deposited silica mask in a single photolithographic step. A second level mask is used to protect the waveguides from the deep mirror etch, and is removed before the subsequent shallow waveguide etch. This self-alignment ensures correct orientation of the mirrors with respect to the waveguides.

CH4:H2 reactive ion etching is used to form the waveguide and mirror recesses, since it is nearly isotropic and can provide profiles which are independent of crystal orientation.

Demultiplexer Performance

By comparing the effect of different combinations of 2-D optical components, the resolution and registration of the 2-D focused images was investigated, and the losses incurred at mirror reflections estimated. No significant deterioration was observed in the image of a 2.5 µm wide source formed by two intermediate focusing mirrors at a total source to image distance of about 2 mm. Also, the coincidence between the image and an integrated waveguide was such that within a measurement accuracy of + 0.3 dB all the optical power in the image was collected by the guide. With a grating interposed between the two focusing mirrors there was some broadening of the image, but only by about 0.7 µm. Losses at each mirror and at the grating were estimated to be about 2 and 3 dB respectively, of which 1 dB could be attributed to lack of perfect verticality. These results all highlight the remarkable lack of distortion in the 2D optical propagation, the uniformity of the MOVPE-grown slab waveguide, and the

precision of the photolithography.

<u>Conclusion</u>

An InP-based opto-electronic integration technology has been developed for 1.5 μ m receivers which reconciles the demands of pin diodes and FETs, and which is sufficiently consistent to successfully produce ICs with many tens of individual components. A receiver sensitivity has been measured at 1.2 Gbit/s which is comparable with that of commercially available hybrid pin/FET receivers.

Initial work on the use of InP-based slab waveguide for a monolithic 2-D grating demultiplexer has been very encouraging. Good optical image formation and good grating resolution has been demonstrated. In addition, fabrication is straightforward. On this basis the design of a satisfactory monolithic demultiplexer and the additional integration of optelectronic and electronic components does not seem an impractical proposition.

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