

**Invited****Future Directions in Materials and Processes for Silicon ULSI Technology**

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New materials and processes are key elements in the continuing evolution of semiconductor technology. Significant improvements in performance can be gained by solving key problems relating to conductors, insulators, and semiconductors. This paper describes some of the strategic directions in the materials and processing areas.

The phenomenal growth of the electronics industry over the last few decades is a direct result of the rapid improvement in performance, density, and cost of semiconductor circuits. The most common example of this dramatic evolution is the dynamic RAM chip. In the last 10 years, the size of a memory cell has decreased by a factor of 30 and the cost per bit has decreased by a factor of 50. The result has been the development of new applications and new markets with an increasing appetite for memory. Underlying this rapid progress are significant advances in materials and processes for silicon technology. Improvements in lithographic techniques alone have been responsible for a factor of 10 reduction in memory cell area in the last 10 years.

Lithography is worthy of dedicated treatment elsewhere, allowing us to focus on the remaining issues in materials and processes. Three basic types of materials are used in silicon technology. Conductors are the key to local and global circuit interconnections. Insulators provide the necessary

isolation of the conductors and serve as the dielectric for capacitors. The semiconductor material itself forms the heart of the transistor. Each of these types of materials requires special processes for use in integrated circuits. In this paper we will consider some examples of future strategic directions in each of the three types of materials.

The development of a process to connect two device contacts with a thin film of aluminum was key to the invention of the integrated circuit by Jack Kilby<sup>1)</sup> and Robert Noyce<sup>2)</sup>. With the addition of some copper to avoid electromigration, aluminum is still used to interconnect circuits. Key process enhancements enabling continued use of aluminum include the ability to reactive-ion-etch the metal and the use of barrier layers to avoid metal penetration and to improve contact resistance. The critical question for future directions is whether aluminum will be replaced with a lower resistivity metal. Copper is generally considered the most likely candidate. As the metal lines become narrower, the lower resistivity of copper

could help reduce RC time constants. Key processes to be developed include conformal deposition and high aspect ratio vias, planarization, etching, and passivation. Questions of adhesion and interdiffusion must also be addressed. If barrier layers and adhesion layers will be required to clad the copper, the resistivity benefit may be reduced and may no longer provide sufficient leverage to offset the additional complexity.

A second type of conductor widely used in silicon technology is that of metal silicides. These alloys have excellent process compatibility and sufficiently low resistivity to make them useful for gate electrodes, source/drain contacts, and local interconnects. Technology evolution dictates the use of thinner silicide films<sup>3)</sup> and shallower source/drain junctions, which require reduced thermal diffusion. Unfortunately, this trend leads to higher silicide resistivity. Rapid thermal annealing has been found to be effective in achieving low resistivity coupled with minimal thermal diffusion and is therefore becoming an essential part of a silicide process.

Insulators play a dual role in silicon technology. They not only isolate conductive regions, but their dielectric characteristics are important in determining capacitance. The FET gate insulator is the best example of the key role played by silicon dioxide. Scaling rules dictate that the gate oxide thickness should continue to decrease in order to improve performance at smaller lateral dimensions. However, the onset of tunneling current will provide a fundamental limit to the extent to which oxide film thickness can be reduced. Recent results<sup>4)</sup> indicate that a 4-5 nm film may be achievable with sufficiently low supply voltage.

Insulating films for storage nodes will require composite or novel materials with high dielectric constants to achieve higher capacitance. For example, Ta<sub>2</sub>O<sub>5</sub> has been used in a recently reported DRAM cell<sup>5)</sup>. This material has a potential dielectric constant nearly an order of magnitude greater than that of silicon dioxide, but significant materials and process challenges remain to be resolved.

At the other end of the spectrum, a very low dielectric constant is necessary for interconnect wiring to minimize both the capacitive coupling of signal lines and the capacitive wiring load. In future technologies, as much as 50% of the on-chip delay may be due to the capacitive wiring load. A reasonable lower bound on the value of the dielectric constant that might be achieved is 2, half the typical value of silicon dioxide. Such a material, most likely a polymer, must meet stringent constraints of mechanical, thermal, and electrical characteristics as well as process compatibility. Low dielectric constant insulators would also provide significant leverage in semiconductor packaging.

Finally, the semiconductor material itself forms the core of the integrated circuit. Perhaps the most fundamental process related to semiconductor material is that of impurity doping, the key to controlling electron density. Ion implantation is currently the most common technique used to achieve shallow junctions. However, two factors will limit its usefulness in the future. First, channeling effects, which become dominant in low energy implants, lead to a deeper dopant profile than desired. These effects occur even with angled implants through a screen oxide<sup>6,7)</sup>. Second, the

thermal cycle required to remove point defects generated by ion implantation is too large to maintain shallow junctions. Novel processes are needed to achieve sharp junctions with shallow profiles.

A promising candidate is that of UHV/CVD low temperature silicon epitaxy<sup>8</sup>). This process has been used to deposit thin layers of doped silicon at temperatures on the order of 500°C, well below that where diffusion occurs. The quality of these films has been demonstrated by the fabrication of high-performance bipolar transistors with both homojunction and heterojunction Si-Ge material<sup>9</sup>). Of particular interest is the fact that the boron is activated as-deposited up to concentration levels well above equilibrium<sup>10</sup>). The dopant profile is extremely abrupt and spreads only due to subsequent thermal cycles. This new material and process may be a key to novel structures in the future. With the ability to deposit epitaxial silicon selectively, additional flexibility will lead to more innovation.

In summary, innovation in materials and processes has been the enabler for the evolution of silicon technology. Today's challenges include the development of new materials and processes for the technology of tomorrow. In particular, the use of low conductivity metals, low and high-dielectric constant insulators, and low temperature semiconductor epitaxy have the potential for real leverage and can be expected to be strategic directions for the ULSI era.

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