Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 849-852 **S-CI-11**

Invited

Cluster Tools for Fabrication of Advanced Devices

Dan Maydan

Applied Materials, Inc.

3050 Bowers Ave.
Santa Clara, California 95054
U. S. A.

Semiconductor manufacturers are showing increasing interest in "cluster tools", or systems that perform sequential, or "integrated", processes within a single, vacuum isolated architecture. Applied Materials' recently introduced second-generation integrated processing system, the Endura^{TM} 5500 PVD, is designed for many new integrated processes. This paper describes cluster tool evolution and design considerations, and discusses present and future applications including integrated CVD dielectric and blanket tungsten processes, sputtered aluminum and barrier metal processes, as well as future applications such as integrated single-wafer epitaxial deposition.

Introduction

Trends in semiconductor device production are instrumental in the evolution of “cluster tools”, which will increasingly enable semiconductor manufacturers to perform sequential or “integrated” processes within individual vacuum systems. The technical reasons for this trend include much better control of microcontamination, increased process consistency, and beyond that, process results that are not possible without sequential processing. Economically, integrated processing offers a path to reducing device fabrication time by cutting the number of separate process steps and, potentially, lowering the chipmakers' cost-per-bit.

Device Trends

Using DRAM memory devices as a gauge, one can see that the progression from 1MB to 64MB involves much increased complexity. Feature sizes will shrink from about 1.2μm to about 0.35μm; mask levels will increase from about 12 to over 20; levels of metallization will increase from today's 2-3; and the number of process steps will more than double, from around 150 to over 350.

To successfully and economically produce 64 MB DRAM chips, the industry needs equipment that will fabricate new and unique structures, and do so with very low levels of particulate contamination. This equipment will have to be extremely reliable, despite increased complexity, and offer a high degree of productivity over a lifetime of several device generations. Applied Materials believes that increasing yield and productivity up to, and beyond, 64MB will require process integration.

Cluster Tool Evolution

In 1987, Applied Materials introduced the Precision 5000 CVD, a single-wafer, multi-chamber system that has become the industry’s most successful multi-chamber design (Figure 1). The long-term strategy behind this design was to use the company’s strength in many different types of processes to ultimately offer a wide range of complementary process chambers on a standard wafer handling unit. In addition to the constantly increasing number of individual CVD and Etch processes offered on the Precision 5000-family of systems, the company also began offering several enabling integrated processes,

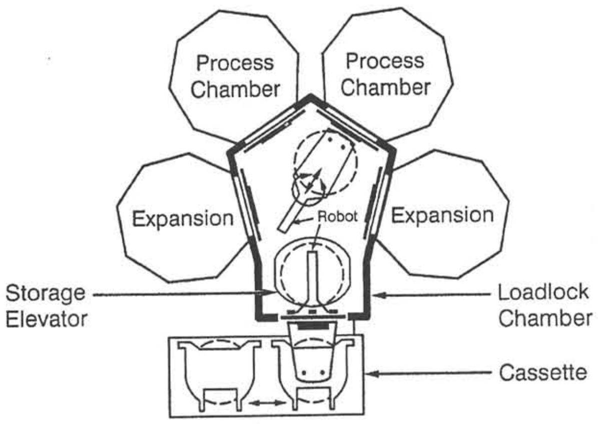

Figure 1. Applied Materials' Precision 5000 system, showing multi-chamber architecture.

including CVD/etch process sequences to perform planarized dielectrics, sidewall spacer (lightly-doped drain) structures, and tungsten contact or via "plugs."

Figure 2 shows a SEM of an integrated intermetal dielectric process; this process in the Precision 5000 is performed automatically using the system software and includes in situ chamber cleaning.

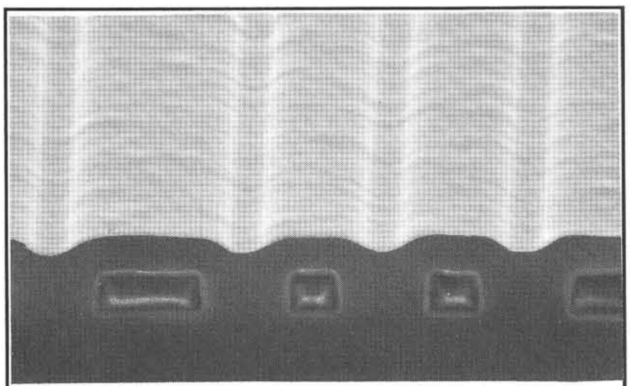

Figure 2. SEM of the integrated intermetal dielectric process as performed on the Precision 5000 CVD.

Figures 3 and 4 illustrate the integrated sequence used to fabricate LDDs, or sidewall spacers. The process deposits a conformal oxide over the gates in the CVD chamber, followed by an anisotropic oxide etch to create the required structure. Recently, the highly successful Precision 5000 WCVD blanket tungsten process has been integrated with a multi-step etchback process to create co-planar tungsten plugs (Figure 5). In all of these examples (which are well-proven and available to customers worldwide), the integrated process completely avoids the need to remove the

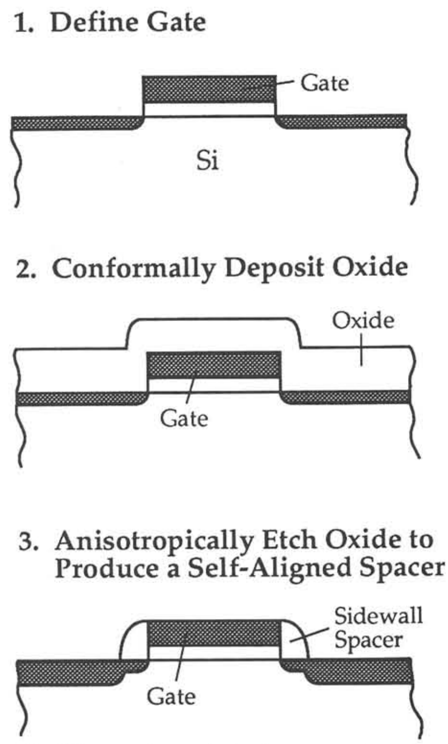

Figure 3. Illustration of the integrated sidewall spacer fabrication process used by the Precision 5000 CVD.

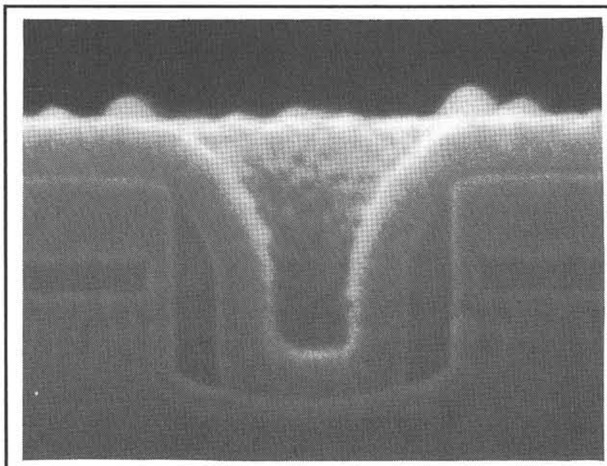

Figure 4. SEM of the integrated sidewall spacer process as performed on the Precision 5000 CVD.

wafer from the system's controlled environment to transport it to a separate etch or CVD system.

The Second Generation of Cluster Tools

In April 1990 Applied Materials introduced the Endura 5500 PVD, which represents the company's, and the industry's, only second-generation cluster system.

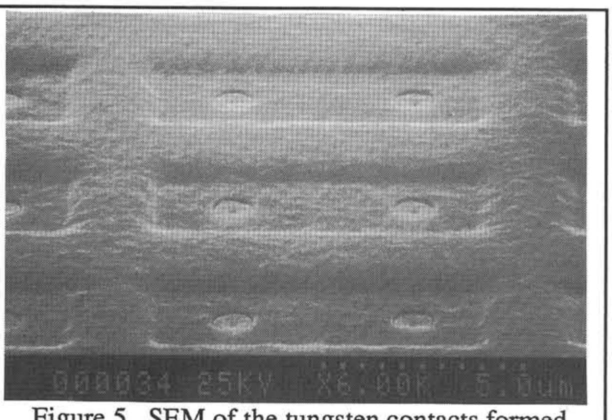

Figure 5. SEM of the tungsten contacts formed using the Precision 5000 WCVD integrated blanket tungsten/etchback process.

The Endura's MasterFab™ concept (Figure 6) involves a staged-vacuum design that gives a tremendous flexibility to combine many different processes with widely different vacuum requirements; these include Physical Vapor Deposition (PVD) of metals, CVD dielectrics and tungsten, etch, epitaxial deposition, Rapid Thermal Processing (RTP), photoresist stripping and others. Integrated into the basic system are chambers for thermal de-gassing of wafers, low-voltage etch pre-cleaning, and wafer cool-down. The staged-vacuum design includes two distinct system sectors that operate at high and ultra-high vacuums, respectively. This allows wafers to progressively pass from 10^{-5} torr to 10^{-9} torr with no more than one order of magnitude difference in vacuum level and ensures against cross-contamination between the chemical and physical processes.

Clearly, as device dimensions shrink, control over film purity and the interfaces between films is becoming extremely critical. The wafer processing environment must be controlled to a much higher degree than ever before, and this means isolating wafers from ambient and performing as many processing steps as possible before exposure to ambient conditions. In addition, new in situ processes that ensure wafer cleanliness and freedom from adsorbed contaminants such as water vapor and atomic hydrogen must be incorporated into the integrated process flow, while maintaining the wafer in a vacuum environment.

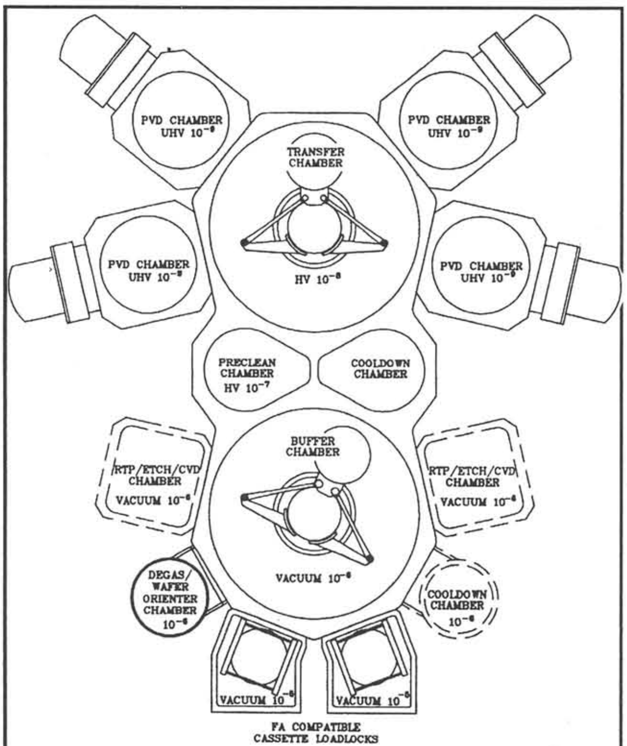

Figure 6. Applied Materials' Endura 5500 PVD system illustration showing the staged-vacuum MasterFab™ architecture designed to integrate both high-vacuum and ultra-high vacuum (10^{-9} torr) processes within one system.

A Systems Approach to Integrated Aluminum Metallization

Investigations into the properties of aluminum PVD have led to the conclusion that only an ultra-high vacuum (10^{-9} torr base pressure) environment offers the control over film purity necessary for the next generation of devices. Very low base pressure is essential to control the level of contaminants that are incorporated into the sputtered aluminum or barrier layer films. The amount of contamination in the film directly affects the conducting metal's grain size and morphology, which influences its ability, in the case of aluminum, to resist electromigration. UHV offers a path to dramatically increased electromigration resistance.

At a base pressure of about 10^{-6} torr, which represents a fairly typical operating pressure regime for many sputtering systems found in fabs today, approximately one monolayer of contaminant atoms is deposited per second (3-5 Å/sec). These contaminants may be water vapor, hydrogen, nitrogen or many other common elements and compounds. Using a base pressure of 10^{-9} torr, this contamination is theoretically reduced to a level of only a few monolayers per hour. Obviously, controlling deposition of unwanted contaminants is essential to ensure the integrity of the aluminum film.

At such high vacuum levels, it is essential that the wafer (and the chamber) be completely free of water vapor, otherwise outgassed molecules become part of the deposited film. The Endura 5500 accomplishes this by means of sophisticated, low-voltage wafer pre-cleaning technology. In addition, low-voltage wafer pre-cleaning effectively controls the undesired native oxide formation that inhibits adhesion and increases contact resistance; thus, pre-cleaning technology will certainly occupy a fundamental place in most future integrated process sequences.

Integrating Barrier Layers

Integrating barrier layers, such as TiW, into the metallization process scheme under controlled vacuum offers many advantages not found in stand-alone applications. The isolation from ambient has a noticeable effect on the Si/TiW interface, offering virtually no spiking and low, uniform contact resistance due to the extremely pure TiW film and interface. The Endura 5500 PVD system's unique source design also offers TiW stepcoverage over 25% in a 0.6-micron feature (Figure 7). A TiN barrier layer plus aluminum deposited in a 0.6-micron contact is shown in Figure 8.

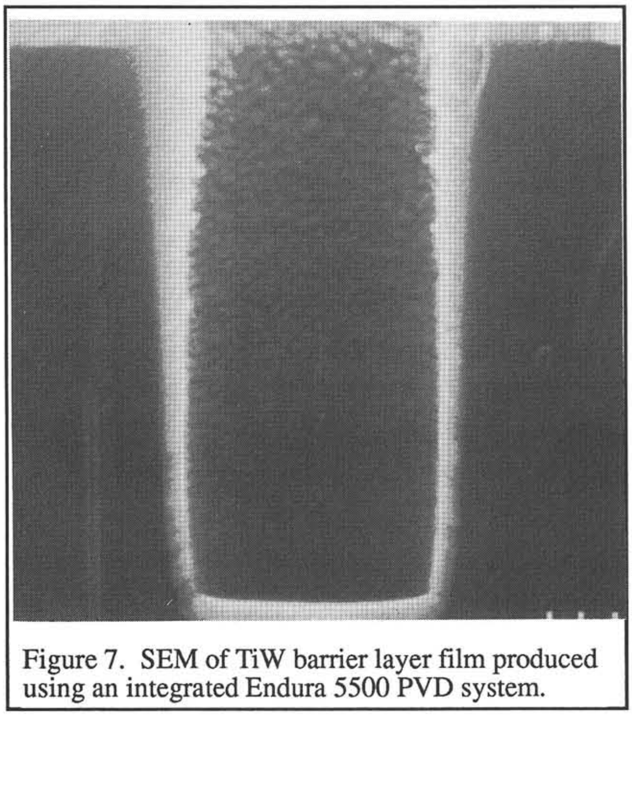

Figure 7. SEM of TiW barrier layer film produced using an integrated Endura 5500 PVD system.

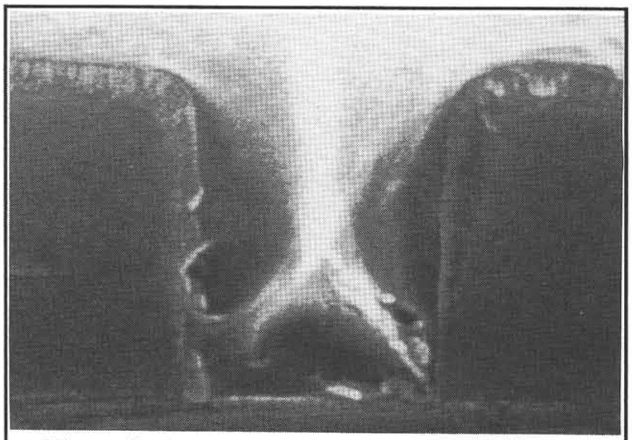

Figure 8. SEM of TiN barrier layer plus aluminum (1% silicon) produced using the Endura 5500 PVD system.

Conclusion

The experience of Applied Materials in integrating advanced semiconductor production processes, involving several complementary disciplines, has been applied to a second-generation metallization "cluster tool" that incorporates many advances in system architecture as well as process technology. Systems that offer the device manufacturer superior process results as well as the potential for long operating lifetimes will necessarily require specialized, yet highly flexible, designs capable of integrating numerous processes within one system.

With several years of experience offering production-worthy integrated processes on the Precision 5000 CVD, Etch and WCVD systems, Applied Materials is investigating numerous additional process sequences that can be integrated within an advanced staged-vacuum architecture. The advantages of these sequential processes include greatly reduced particle contamination for higher yield and productivity, fewer process steps for shortened cycle time for completed device structures, and the potential to lower the cost-per-bit through at least the 64MB device generation.