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Invited

The Technology Trends in Sub-0.5 μm Bipolar

Tak H. Ning

IBM Research Division
Thomas J. Watson Research Center
Yorktown Heights, NY 10598 U.S.A.

The technology trends in scaling silicon bipolar towards sub-0.5 μm dimensions are projected by examining the delay components in the power-delay characteristics of bipolar logic circuits. The directions for technology developments include (i) further reduction of the parasitics of the trench-isolated "double-poly" self-aligned device structure, including the use of dieletric-filled deep trenches, shallow trenches, and emitter-trench butting, (ii) further optimization of the vertical device profile, including reduction of the emitter junction depth, and (iii) emphasis on minimizing the base-push-out effect by optimizing the collector doping profile while maintaining adequate E-C punch-through voltage. The new and exciting opportunities offered by heterojunction structures, epitaxy base, high-performance pnp, and low-temperature circuit operation are also discussed.

I. Introduction

Over the past few years, the trench-isolated self-aligned silicon bipolar technology has evolved to the point of broad application in high-speed systems, especially in high-end computers. This evolution is not unexpected [1]. Figure 1 shows the reported ECL ring-oscillator speeds of these self-aligned bipolar devices, plotted as a function of the emitter width. It clearly shows that these devices are scalable down to at least about 0.3 μm emitter width.

In this paper, the technology issues for realizing the full potential of sub-0.5 μm bipolar are discussed. By examining the technical challenges as well as the new opportunities offered by recent advances in materials and processes, certain directions or trends in technology development should become apparent.

II. Circuit Delay Components

Figure 2 illustrates the log delay vs. log power of a typical ECL circuit. The delay is dominated by three components, namely the capacitance component, the transit-time component which is determined mainly by the intrinsic device profile, and the base-push-out component which is a strong function of both the device current density and the collector doping profile. In bipolar scaling [2], the device current density increases rapidly. It is therefore clear that the trends in sub-0.5 μm bipolar technology development continue to be the reduction of both the capacitance and transit-time delay components, with simultaneous emphasis on minimizing base-push-out effects.

III. Base-push-out Effects and Collector Design

One of the rules to follow in bipolar scaling is to minimize base-push-out effects [2]. Base push-out can be minimized by reducing the collector epi thickness and/or increasing the collector doping concentration N_C. Figure 3 shows the effect of collector epi thickness on the delay of a typical circuit, first reported by Tang et al. [3]. At low currents, the thick-epi devices are faster because of the smaller B-C junction capacitance. However, at high currents, base-push-out effect limits the device speed, and the thin-epi device is faster.

For a given collector epi thickness, base push-out decreases with increasing N_C. Figure 4 shows the f_T -I_C results reported by Patton et al. [4]. It clearly shows that base push-out due to N_C being too low can easily limit the peak f_T.

The pedestal collector [5, 6] is certainly the preferred scheme for minimizing base push-out. In this scheme, N_C is increased only beneath the emitter region, thus minimizing base push-out without increasing the extrinsic B-C junction capacitance [7, 8].

To minimize base push-out, N_C should be a few times larger than J_C/qv, where J_C is the collector current density and v is the carrier velocity. Thus, for J_C = 1 mA/μm^2, and v = 10^7 cm/s, N_C should be larger than $10^{17} cm^{-3}$. This estimate is consistent with the data shown in Figure 4.

As the collector epi thickness is reduced and/or N_C is increased to minimize base push-out, the B-C junction avalanche breakdown voltage, BV_{CBO}, decreases. The holes (in the case of npn) generated in B-C avalanche add directly to the base current, but in a reversed flow direction, and could cause very large changes in the base current. Therefore, there is a device design conflict between minimizing base push-out and minizing B-C junction avalanche [9].

Lu and Tang proposed to resolve this design conflict by sandwiching an i-layer between the base and the collector regions [10]. Figure 5 is one of the designs discussed in Ref. 10. Using low-temperature epitaxy for forming both the i-layer and the intrinsic-base layer, Comfort et al. [11] demonstrated that it is indeed possible to increase the B-C junction avalanche voltage with minimal decrease of the device peak f_T.

IV. Transit-time Delay Component and Emitter Engineering

The transit-time is the sum of the emitter-charge storage time, the base transit time and the collector transit time. For base widths of 50 mm or thinner, quasi-ballistic transport through the neutral base region and velocity overshoot at the B-C junction are expected [12]. Also, the collector transit time could be significantly larger than the base transit time, again suggesting the importance of collector design [12].

Heterojunction devices in the form of wide-band-gap emitters and/or narrow-band-gap base regions could have a much smaller transit-time delay component. The recent advances in SiGe-base technology have been particularly exciting [4, 13]. In this case, the heterojunction structure minimizes the emitter charge-storage time, and the built-in drift field in the graded-bandgap base reduces the base transit time, resulting in a peak f_T of 75 GHz, almost twice that of a Si-base device.

It is now possible to replace ion implantation by epitaxy deposition for forming the intrinsic-base region [14, 15]. Conceptually, epitaxy deposition could give a thinner and more rectangular base profile than ion implantation, which normally gives a Gaussian profile. In order to maintain a tight distribution in BV_{CEO} values, the emitter junction depth, X_{je}, should be small compared with the base width [6]. This important point is illustrated in Fig. 6, which shows that for a given base junction depth, the final integrated base doping, hence the BV_{CEO} value, decreases with X_{je}, more rapidly for a Gaussian base profile than for a rectangular base profile.

Figure 7 is a plot of measured BV_{CEO} vs. f_T data compiled from several recent publications. It shows that the high f_T devices could suffer from BV_{CEO} being too low, and that the epitaxial-base devices could have higher BV_{CEO} than the implanted-base devices, consistent with the above discussion. However, it is also clear from Figure 6 that for near-zero emitter depths, the difference in BV_{CEO} control between implanted and epitaxy bases could be negligibly small.

V. Device Structures and Capacitance Delay Component

Figure 8 shows the schematics of two commonly used trench-isolated self-aligned bipolar transistors (shown here with shallow trench). ECL ring-oscillator delays of about 30 ps have been demonstrated with these device structures [8, 16, 17]. The symmetrical or SICOS structure [17] shown in Fig. 8b conceptually should give lower C_{CB} than the structure shown in Fig. 8a. However, the difference could become negligibly small for emitters butted against shallow trench.

The development of shallow trench for field oxide has been driven by high-density DRAM applications [18]. Shallow trench has been applied to self-aligned bipolar as well [16, 19]. Emitter butting can further reduce the B-C junction area, and hence the capacitance delay component, substantially [6, 20]. With shallow trench and emitter butting, the transistor should have comparable collector and emitter areas, and therefore good current gain in upward operation, similar to the SICOS structure.

Another trend is to replace polysilicon by oxide [6] or BPSG [8] for filling the deep trenches. Such dielectric fill allows trench widths to be reduced to submicron dimensions.

VI. New Opportunities

(a) Heterojunction Structures and Epitaxial Base

The recent breakthroughs in wide-bandgap SiC-emitter [15] and narrow-bandgap SiGe-base [4, 13], as well as simple epitaxy-base [4, 11, 15] technologies provide new degrees of freedom for minimizing the transit-time delay components, as discussed in Section IV above. With heterojunction structures, devices with peak f_T of greater than 100 GHz should be possible.

(b) Complementary Bipolar

It has been shown that vertical pnp transistors can be as fast as vertical npn transistors [19]. The process for integrating vertical npn and vertical pnp transistors, however, is rather complex, primarily due to isolation problems.

SOI, with its insulating substrate, is ideal for integrating lateral npn, pnp, and CMOS devices on the same chip. To drive the development of this technology, inventions of complementary bipolar circuits with little or no standby power dissipation and small (about 500 mV) logic swing are needed.

(c) Low-Temperature Bipolar

As the base doping concentration is increased in bipolar scaling, the difference between the emitter and the base bandgaps decreases, making the current gain less sensitive to temperature. Consequently, submicron scaled bipolar devices and circuits work very well at low temperatures. Heterojunction structures, as well as pseudo-heterojunction structures [21], can further improve the current gain at low temperatures.

To first order, the logic swing, and hence the power dissipation, can be scaled with the operating temperature. Figure 9 shows that the power-delay product of ECL circuits could be reduced by low-temperature operation [22].

VII. Summary

With polysilicon emitter, self-aligned silicon bipolar devices are scalable down to at least 0.25 μm emitter width. The recent developments in epitaxy base, SiC emitter, and SiGe base give new degrees of freedom in processing, suggesting the possibility of scaling far beyond 0.25 μm. For such small dimensions, collector profile design is critical, and could easily become more important in determining device and circuit performance than the emitter and base profile designs.

The parasitic capacitance component can be further reduced by using dielectric filled deep trenches, shallow-trench field oxide, and processes that allow emitter butting.

Complementary bipolar and low-temperature bipolar are clearly within reach, from fabrication technology point of view. More study, particularly in circuits, is needed before the potentials of these technologies are clear.

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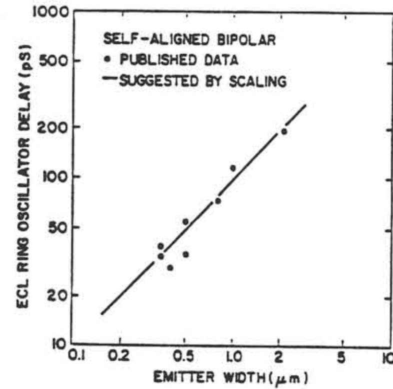

Fig. 1 Published ECL R.O. delays plotted as a function of emitter width for double-poly self-aligned bipolar devices.

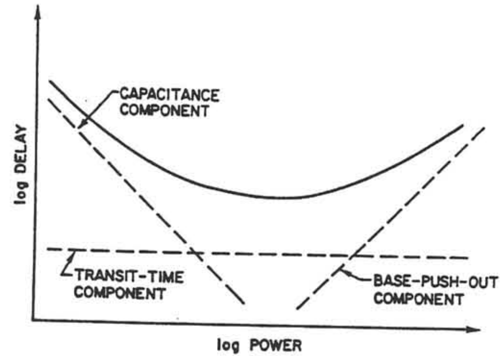

Fig. 2 Log delay vs. log power plot of a typical ECL circuit.

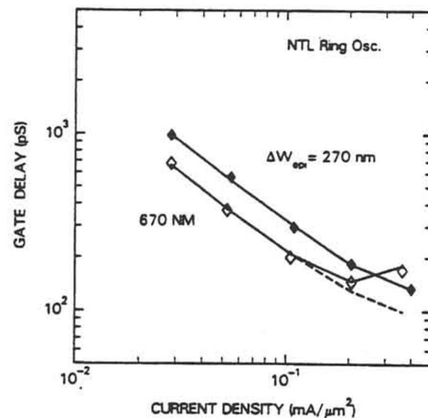

Fig. 3 Measured NTL R.O. delay vs. current density for two epi thicknesses. (After Tang et al., Ref. 3)

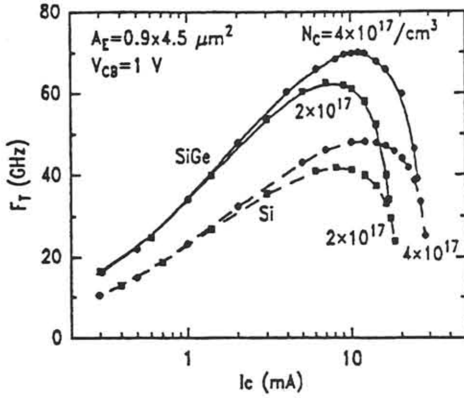

Fig. 4 Measured f_T vs. collector current. (After Patton et al., Ref. 4)

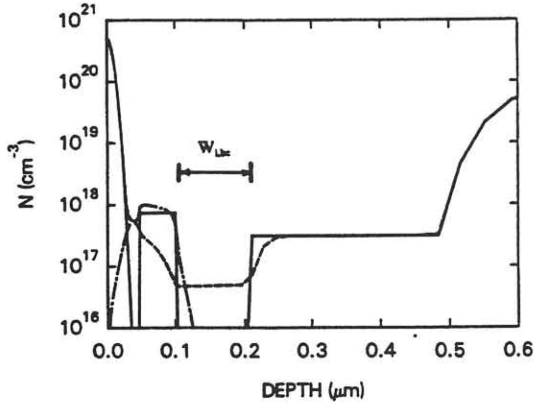

Fig. 5 Doping and carrier profiles for a transistor with a 100nm i-layer sandwiched between base and collector. (After Tang and Lu, Ref. 10)

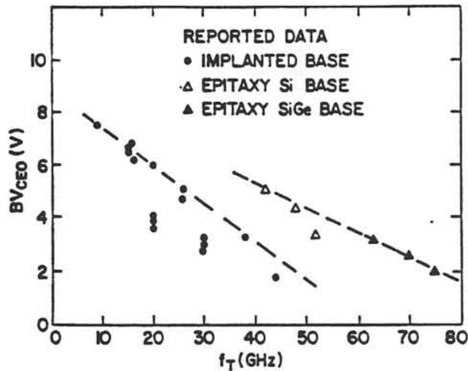

Fig. 7 Some recently published BV_{CEO} vs. f_T data.

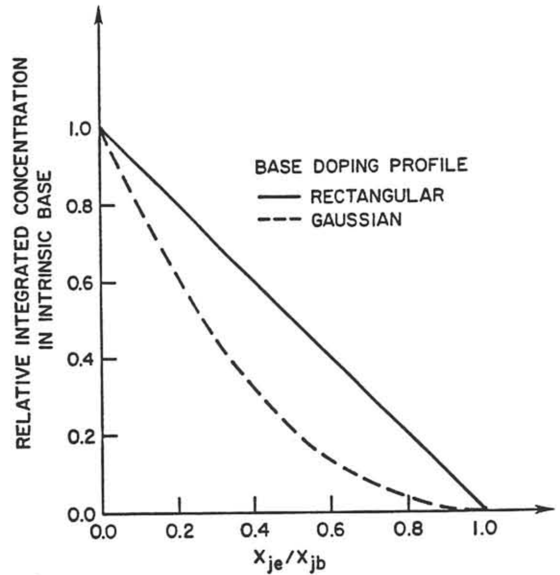

Fig. 6 Calculated relative integrated base doping vs. emitter/base junction depth ratio.

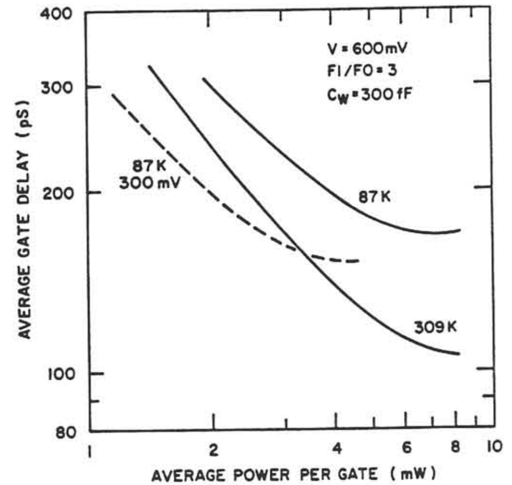

Fig. 9 Simulated delay vs. power for an ECL circuit operating at 309K and 87K. (After Cressler, Ref. 22)

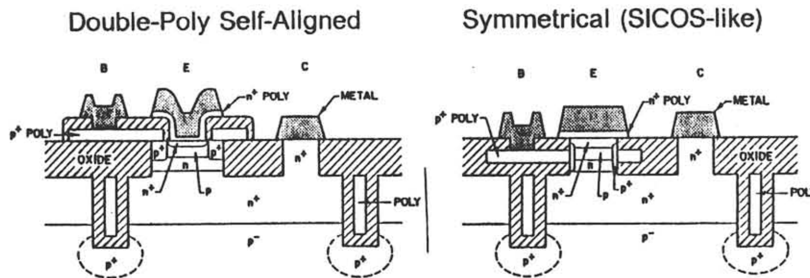

Fig. 8 Schematics of two commonly used self-aligned bipolar device structures, shown here with deep and shallow trenches.