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Process Technologies for Advanced Si Bipolar Devices

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In this paper we present breakthroughs in Si bipolar transistor process technology, with emphasis on the emitter and base. We discuss the limitation of the conventional poly-Si emitter and demonstrate using a heterojunction at the emitter-base junction to overcome it. We show how the SiCx-widegap-emitter lowers base resistance and produces adequate current gain. We introduce a technique using low-temperature Si epitaxy to fabricate a thin, highly doped base. This technique enables the delay associated with excess minority carrier charge in the base to be reduced to the sub-picosecond range. We emphasize that other delay components such as collector-base depletion layer delay should be decreased, while maintaining a reasonable collector-emitter breakdown voltage.

1. Introduction

The realization of high-speed, large-capacity digital communication and computer systems largely depends on the development of high-speed semiconductor devices. The bipolar transistor's exponential I-V characteristic gives it the highest transconductance among the semiconductor devices and results in the bipolar transistor's excellent wiring capacitance drive capability.

The progress of high-speed bipolar transistors can be illustrated using the switching delay of the ECL ring oscillators. Figure 1 plots gate delay data collected from several industrial laboratories[1] and shows that gate delay has reached into the sub 30 ps range. These short gate delays are due to advanced process technologies such as the poly-Si emitter, the self-aligned base contact, the low-energy boron ion implantation, the pedestal collector, and the deep trench isolation. Most of these features are requisite for sub 30 ps gate delays. For further improvement, we will need breakthroughs in the above techniques.

In this paper, we propose breakthrough emitter and base fabrication techniques for advanced Si bipolar transistors.

2. Advanced Si bipolar process

2.1 Emitter fabrication process

Conventional poly-Si emitters have the following limitations: 1) emitter junction depth is limited to about 30 nm in order to separate the emitter-base space charge region from the interface[2]. To limit emitter charge storage, the mono-Si emitter region should be made as shallow as possible. 2) To reduce the delay associated with excess minority carrier charge in the base and base resistance, and to avoid emitter-collector punchthrough, a thin, highly doped base is desirable. But, maximum base doping is limited by decreased current gain and the onset of a forward-bias tunneling current. 3) In consideration of very thin base matching, impurity diffusion from the emitter material into the base to fabricate a mono-Si emitter should be avoided

for precise process control. The desirable emitter material is that which works well as an emitter as deposited. Considering the above limitations of the poly-Si emitter, a heterojunction at the emitter-base junction is desirable. We have been investigating a SiC-widegap emitter[3]. Low-temperature grown (700°C), non-epitaxial SiCx is used as a wide-gap emitter material. To suppress recombination current, we added fluorine to terminate the dangling bonds at the heterojunction. A fluorinated heat-resisting amorphous Si alloy whose dangling bonds were terminated by fluorine has been used for low-cost solar cells[4].

Figure 2 shows the common-emitter output characteristics of the HBT. The base was 50-nm thick with a carrier concentration of 10^{19} /cm^3. We made the base by low-temperature Si photoepitaxy[5]. The SiCx film was 50-nm thick and had a carrier concentration of 10^{19} /cm^3. The current gain was 80, about 5 times larger than that of nonfluorine-doped-SiCx-HBTs. Despite the very thin base, the Early voltage was over 100 V. The measured pinch resistance was extremely low: 1.75 kΩ/square. Using a base carrier concentration of 10^{19} /cm^3, and an epitaxial base thickness of 50 nm, we calculated the sheet resistance to be 1.7 kΩ/square. From the above results, we think that the base doping profile was little disturbed by the emitter deposition process. A current gain of 80 and a pinch resistance of 1.75 kΩ/square is attainable only by using a heterojunction at the emitter-base junction.

Figure 3 compares the current gain of the HBT and a conventional poly-Si emitter homojunction transistor. Except for the emitters, the two transistor have the same structure. The SiCx emitter's current gain is four times greater and less collector current dependent than that of the homotransistor.

From the above results, it can be seen that the limitations of a poly-Si emitter can be overcome by using the SiCx emitter.

2.2 Thin base fabrication process

The effect of the base resistance on circuits used for high-performance system must be minimized. The self-aligned base contact virtually eliminates extrinsic base resistance. The intrinsic base doping should be increased to keep a low intrinsic base resistance and to avoid emitter-base punchthrough, while reducing the base thickness. Application of conventional techniques for intrinsic base implantation leads, however, to severe problems due to the channeling of boron ions in the Si lattice, and it is very difficult to achieve a thin, highly doped base.

We have been investigating a thin base fabrication technology using low-temperature photoepitaxy[6]. The epitaxially grown base transistor (EBT) has an in-situ boron-doped epitaxial base layer. The base doping concentration and the base width can be optimized separately by the epitaxy. The box profile of the base dopant is desirable because it minimizes the base width, while maintaining the required base Gummel number to achieve an acceptable punchthrough voltage. Conventional epitaxial growth at around 1000°C cannot fabricate a very thin epitaxial layer because of auto-doping and solid-state diffusion. Photoepitaxy enables us to produce a very thin, highly doped layer because of its low growth temperature of around 600°C. Figure 4 shows an example of a thin base profile achieved by photoepitaxy. The base width is 65 nm and the peak base doping concentration is 10^{19} /cm^3.

Figure 5 shows the cut-off frequency of the EBT versus collector current characteristics. The test device consists of

20 parallel 0.3 μm x 10 μm^2 transistors. The base is around 50 nm thick with a carrier concentration of $3x10^{18}$ /cm^3. The cut-off frequency of 30 GHz is obtained with a V_{CE} of 3 V. The delay associated with the excess minority carrier charge in the base can be reduced to the sub-picosecond range with this epitaxial base technology.

2.3 Collector and isolation fabrication process

The recent rapid increase in a cut-off frequency is mostly due to high collector doping levels. However, this leads to radically decreased collector-emitter breakdown voltage (BV_{CEO}). Figure 6 plots cut-off frequency versus BV_{CEO} data collected from recent published papers. The cut-off frequency increases due to the suppressed Kirk effect, the reduced collector-base depletion layer delay, and the reduced excess minority carrier charge in the base. Device design for a reasonable BV_{CEO} while keeping a high cut-off frequency is an urgent issue. One possible way to lower the base-collector junction field and to increase BV_{CEO} is to insert a thin i-layer[7].

Deep trench isolation has reduced collector-substrate capacitance and the area occupied for the isolation, allowing a reduction in device area and the associated parasitic capacitance. A natural extension of this is a device structure completely surrounded by dielectric. A structure using bonded SOI is currently being researched[8].

3. Conclusion

We have presented advanced Si bipolar process technologies with emphasis on the emitter and base. We showed the SiCx-emitter reduced pinch resistance to 1.75 kΩ/square and produced adequate current gain. Low-temperature Si epitaxy was shown to be effective to fabricate a thin, highly doped base. They require still technological art, however, they open up chances for super-performance bipolar VLSI device.

Acknowledgement

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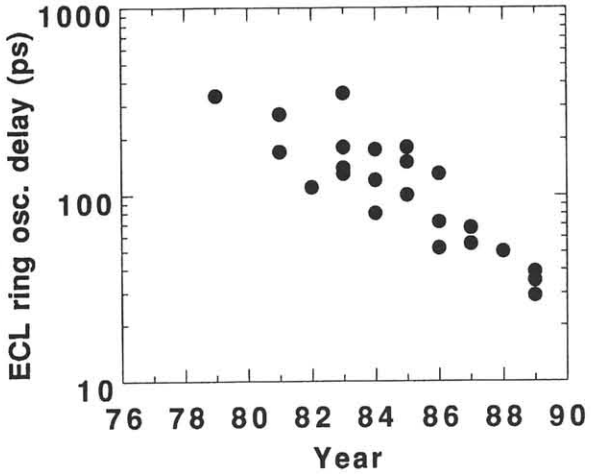

Figure 1 Gate delays of ECL ring oscillators

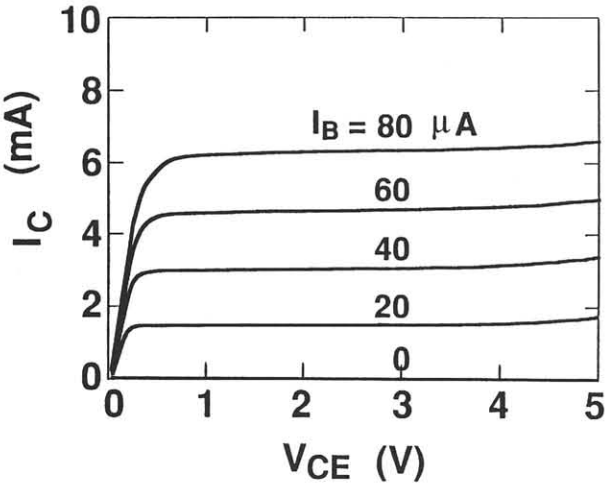

Figure 2 Common-emitter output characteristics of the SiCx-emitter-HBT

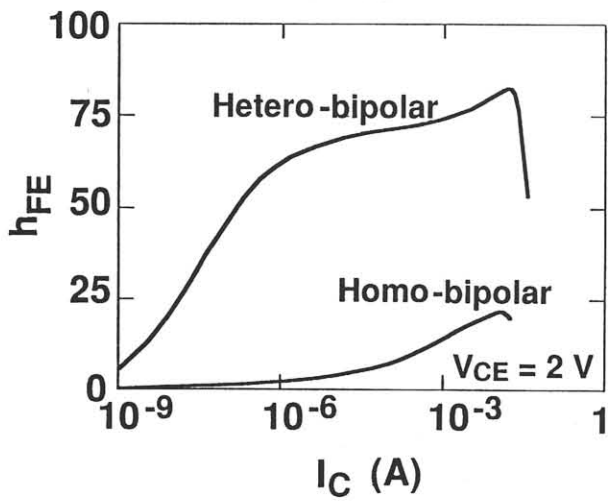

Figure 3 Current gain of the HBT and a conventional poly-Si emitter homojunction transistor as a function of the collector current

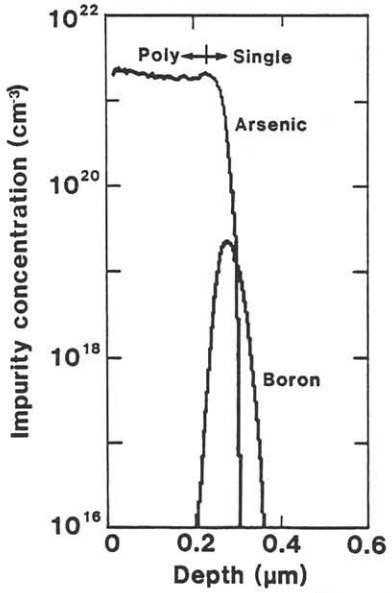

Figure 4 SIMS depth profile of the intrinsic transistor region.

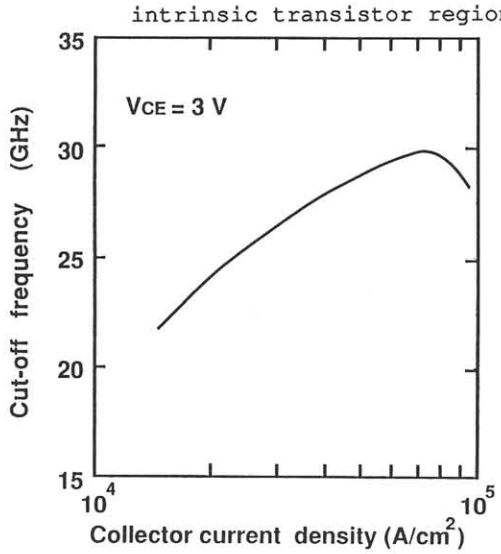

Figure 5 Cut-off frequency of the EBT versus collector current

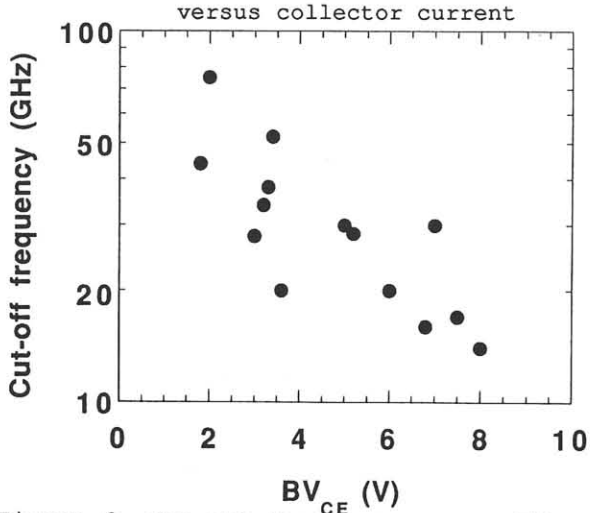

Figure 6 Cut-off frequency versus BV_{CEO} collected from recent published papers