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Invited

Physical Limitations of Ultra Small MOSFETs —Constant Energy Scaling and Analytical Device Model—

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An analytical device model for ultra small MOSFETs is proposed, in which velocity overshoot effect is taken into account. As a proper voltage scaling guideline for MOSFETs with channel length from 1 μm down to sub-tenth μm, we propose "constant energy scaling rule," in which the maximum electron energy at the drain edge is kept constant from the view point of long term reliability of ultra small MOSFETs. The constant energy scaling is derived by taking account of non local carrier heating effect due to finite energy relaxation time. Investigation of device and circuit performances under the constant energy scaling reveals that both device performance and delay time are improved even in sub-tenth μm range.

Introduction

Current VLSI fabrication technology has progressed rapidly and is pushing toward deep submicron dimension devices. In such small devices, high field effects become more pronounced such as non-stationary transport and hot-carrier induced degradation of devices. In order to realize high reliable small MOSFETs with keeping minimum circuit delay, traditional quasi-constant voltage scaling theory[1)] may not be adequate for below half-micrometer region. To make a proper voltage scaling guideline from a view point of device reliability, one should know physical parameters which affect average electron energy. Because of the finite energy relaxation time, the electron energy in ultra small MOSFETs is not a function of the local electric field but of the electric field distribution; non-local carrier heating effect. Therefore, upper voltage of power supply should be determined by taking into account electron energy. In Section 1, a new device model including velocity overshoot effect is presented. In Section 2, we propose a new voltage scaling guideline for ultra small MOSFETs which assures high reliability without losing device performance.

1. Analytical device model

1.1 Physics of carrier transport

From the Boltzmann transport equation, the following *momentum conservation equation* is obtained

$$v_d = \frac{\tau_m}{m^*}\left[-qE - \frac{2}{3n}\nabla(n\cdot\varepsilon)\right]. \quad (1)$$

where τ_m is momentum relaxation time and ε is average electron energy. From the above equation, one finds that

$$v_d = v_d^o\left(1 + \frac{2}{3q}\cdot\frac{d\varepsilon}{dE}\cdot\frac{1}{E}\nabla E\right) - \frac{D}{n}\cdot\nabla n \quad . \quad (2)$$

In the drain depletion region of MOSFETs where electric field is high enough to cause velocity saturation, drift velocity in the drain depletion region becomes[2)]:

$$v_d = v_d^o\left(1 + \frac{\delta}{E}\cdot\frac{dE}{dx}\right) \quad . \quad (3)$$

where v_d^o is drift velocity under a homogeneous electric filed and $\delta=(2/3)(d\varepsilon/qdE)$. At high electric field region, δ becomes $(2/3)(v_{sat}\tau_e)$ in the first order of approximation, where v_{sat} and τ_e are saturation velocity and energy relaxation time, respectively. Furthermore, the Boltmann equation multiplied by the kinetic energy $(v^2/2m^*)$ yields the following *energy conservation equation*:

$$\frac{5}{3}v_d\cdot\nabla\varepsilon = -qv_d\cdot E - \frac{\varepsilon - \varepsilon_o}{\tau_e} \quad (4)$$

1.2 Electrical characteristics of MOSFETs

In MOSFETs operating under saturation condition, the electric field in the drain depletion region is approximately given by[3)]

$$E(y) = E_s \cosh\left(\frac{y}{\lambda}\right) \quad (5)$$

where E_s is saturation field and y is measured from the pinch off point. Substituting Eq.(5) into Eq.(3), the overshoot drift velocity on the average in the drain depletion region is

$$v_s = v_{sat}\left(1 + \frac{v_{sat}\tau_e}{3\lambda}\right) \quad (6)$$

Since all physical parameters except λ in Eq.(6) are constant, the overshoot drift velocity in the pinch off region becomes only a function of gate oxide thickness t_{ox} and junction depth x_j because of $\lambda^2 = 3t_{ox}x_j$. By equating the saturation current and the unsaturated current at the pinch off point, electrical characteristics of ultra small MOSFETs where velocity overshoot occurs can be expressed as:

$$I_{dsat} = \frac{W}{L} C_{ox}\mu_{eff}\left(V_g - V_t - \frac{V_{ds}}{2}\right) \cdot \frac{V_{ds}E_s L}{V_{ds} + E_s(L - \Delta L)} \quad (7)$$

In Eq.(7), the saturation voltage, V_{ds}, and the length of pinch off region, ΔL, are calculated self-consistently from the following two equations[5)].

$$V_{ds} = \frac{E_s(L - \Delta L)(V_g - V_t)}{E_s(L - \Delta L) + V_g - V_t} \quad (8)$$

$$\Delta L = \lambda \sinh^{-1}\left(\frac{V_d - V_{ds}}{\lambda E_s}\right) \quad (9)$$

From the relation given by Eq.(3), saturation field in Eq.(7) is defined as

$$E_s = \frac{2v_{sat}}{\mu_{eff(E_\perp)}}\left(1 + \frac{v_{sat}\tau_e}{3\lambda}\right) \quad (10)$$

where $\mu_{eff(E_\perp)}$, low field mobility, is a function of vertical electric field[4)], $E_\perp$.

Eq.(7) is quite similar to the velocity saturation model[3)] originally proposed by Sodini *et al.* but is further extended to the MOSFETs in which velocity overshoot occurs in the drain depletion region. It should be noted that the analytical model cannot be used for the device in which appreciable velocity overshoot occurs at the source edge.

1.3 Maximum electron energy

In MOSFETs, electric field along the channel grows almost exponentially towards the drain as given by Eq.(5). Electrons in the channel, therefore, gain kinetic energy from the applied electric field and become hot. It should be emphasized that average electron energy is no more function of local electric field: because of the finite energy relaxation time and very high field gradients in a very short channel device, average maximum energy ε_{max} at the drain edge never reaches its steady-state value, which is actually reduced compared to longer channel devices at the same maximum electric field. The maximum electron energy near the drain edge is evaluated by substituting Eq.(5) into Eq.(4) followed by integration.

$$\varepsilon_{max} = \varepsilon_o + qv_s\tau_e E_{max}\left(1 + \frac{5v_s\tau_e}{3\lambda}\right)^{-1} \quad (11)$$

where Emax is the maximum electric field at the drain edge and ε_o is thermal electron energy. Compared with the conventional expression, the maximum electron energy is reduced by a factor of $(1+5\tau_e v_s/3\lambda)^{-1}$ due to non-local carrier heating effect.

2. Discussion

2.1 Device characteristic

To calculate electrical characteristics of ultra small geometry devices using Eqs.(7)~(10), saturated velocity of electrons in the pinch off region is assumed to be 0.7×10^7 cm/sec: lower saturation velocity in silicon surface layer is reported in the literatures[6-9)] (v_{sat} = 0.40 ~ 0.92×10^7 cm/sec). It is only natural that additional scattering mechanisms involved at the Si/SiO_2 interface reduce saturation velocity. However, this is not the case for impurity scattering, which reduces low field mobility but not saturation velocity because high energy electrons are rarely scattered by impurity atoms. In addition, there exist two other factors affecting the drain current of ultra small MOSFETs; (1)parasitic resistance such as contact and sheet resistances and (2)mobility degradation due to vertical electric field.

The IR drop across the series resistance becomes a non-negligible fraction of the applied voltage because the drain current per unit width increases with miniaturization. In practice, the parasitic resistance actually increases over scaling to smaller dimensions. Therefore, overall transconductance including the effect of parasitic resistance should be used as a measure to evaluate device performance of ultra small MOSFETs. Fig.1 shows the calculated device characteristics with and without parasitic resistance. The figure clearly demonstrates that the source and drain parasitic series resistances play an important role limiting the device performance for ultra small MOSFETs.

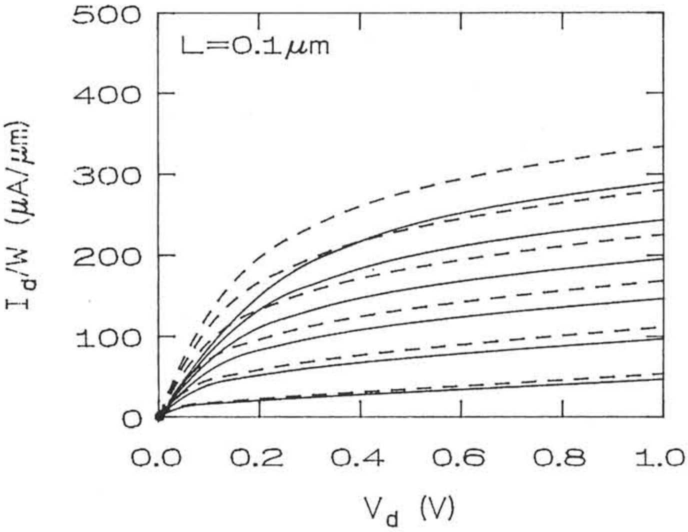

Fig.1 Calculated device characteristics for L=0.1 μm MOSFET with (solid lines) and without (dashed lines) parasitic resistance at room temperature. The parasitic resistance is assumed to be 400 Ω·μm.

Moreover, the transconductance shown in Fig.2 increases at low gate voltage followed by reaching the peak and then decreases with increasing gate voltage. Thus negative differential resistance characteristics becomes pronounced especially for short channel devices operating at low temperature. It is the degradation of low field mobility at high gate voltage that gives rise to the negative differential resistance. The calculated characteristics taking into account both the reduction of low field mobility and the resistances agree well with the experimental data[11], which confirms the validity of the new model given by Eqs.(7)~(10).

2.2 Guideline for voltage scaling

In deep submicron devices, field strength is not the relevant physical parameter to describe average electron energy. Indeed, reduction of hot-carrier induced substrate current even at the same electric field has been reported in sub-150 nm channel length devices[10]. Intuitively, average carrier energy should not exceed the applied voltage. This is not the case when the

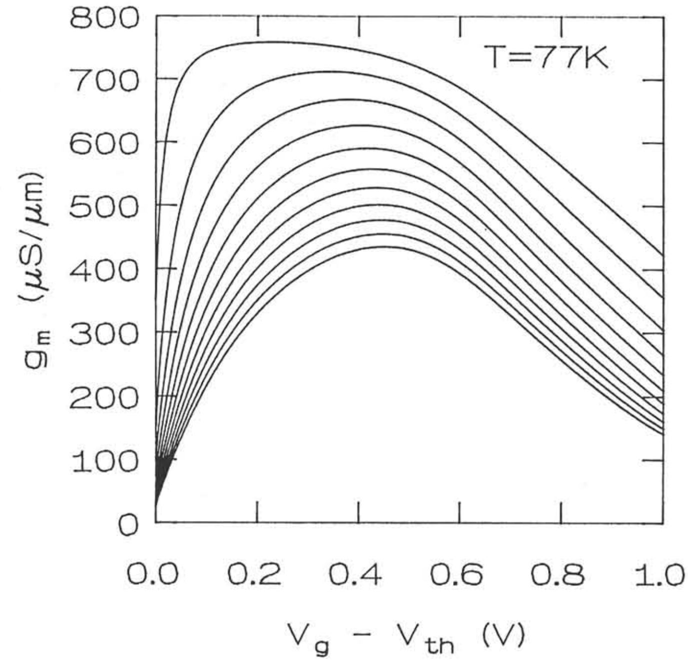

Fig.2 Calculated trasconductance as a function of gate voltage. The decrease of transconductance at high gate voltage originates from the reduction of low field mobility due to vertical electric field.

average electron energy is a function of electric field. : In the limit of $\lambda \to 0$, Eq.(11) predicts that the maximum energy of electrons never exceeds the applied voltage rather than up to 60 % of the applied voltage because E_{max} is inversely proportional to λ. Such non-local carrier heating effect is pronounced when the characteristics length, λ, is comparable to the energy loss distance, $v_{sat}\tau_e$.

In the following discussion, we consider conventional MOSFETs to make the analysis simple. From a view point of device reliability, it is desirable to keep the maximum electron energy as low as possible but lower voltage gives rise to significant circuit delay. Therefore, pertinent guideline for voltage scaling is required. We propose a new voltage scaling rule called *Constant Energy Scaling,* in which the maximum energy ε_{max} is set an allowable maximum value from a view point of device reliability. The allowable maximum energy should be a universal value (~0.4 eV) regardless of device dimension and device structures. Fig.3 shows allowable maximum applied voltage as a function of channel length. All of the device parameters except gate oxide thickness are miniaturized with the same scaling constant.

Dopant concentration at the channel region is determined so as to avoid punchthrough, that is, to satisfy the Brews's short channel criterion[12]. Fig.3 indicates that with decreasing the device size, the supply voltage should be reduced more rapidly than the predicted value from the quasi-constant voltage scaling theory. If one uses the conventional geometry scaling rule, gate oxide thickness would be 3 nm at 0.1 μm resulting in appreciable leakage current due to direct tunneling. To avoid the leakage current, the scaling of gate oxide thickness should be relaxed. If one uses two-third power of scaling factor to gate oxide scaling, the minimum channel length further extend down to 0.06 μm as shown in Fig.3.

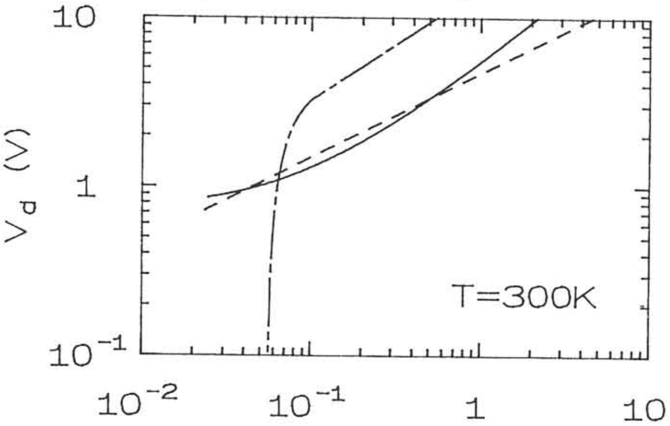

Fig. 3 Allowable maximum supply voltage as a function of channel length based on constant energy scaling (solid line), quasi-constant voltage scaling (dashed line). Device scaling is limited by oxide leakage at L=0.06 μm (dash-dot line). All the geometry parameters except oxide thickness are scaled with scaling factor K, while oxide thickness is scaled with $K^{2/3}$: Oxide thickness and junction depth of MOSFET with L=0.5 μm are t_{ox}=15 nm and x_j=0.15 μm, respectively.

Conclusions

We proposed a new scaling rule called "constant energy scaling" which assures high reliability of MOSFETs without reducing circuit and device performance. In addition, a new device model including velocity overshoot effect was also proposed to evaluate current-voltage characteristics of ultra small MOSFETs. According to the conventional scaling rule, MOSFETs with channel length of 0.1 μm was found to be the minimum dimension. However, the minimum dimension would be further reduced by relaxing the scaling to the gate oxide thickness.

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