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Invited

Advanced Process Features for High Density DRAMs

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The evolution of DRAM technology is overviewed with a future perspective including the 64M generation. The tree of cell structures starting from the basic threedimensional approaches trench cell and stacked capacitor cell is discussed. For capacitor dielectric among several alternatives the widely used ONO will probably suffice for 16M and 64M devices. The reduction of the one transistor cell size circumventing lithographic tolerances will be assisted by various selfalignment techniques such as a selfaligned bitline contact. Finally the limitations of current interconnect and contact metallisations schemes as well as possible solutions are addressed.

1. INTRODUCTION AND OVERVIEW

DRAMs have widely been considered as the main technology drivers for silicon ICs with respect to process innovations, fine patterning technology and manufacturing culture. This technology overview covers the cell structures (2.), capacitor dielectric (3.), selfaligning techniques (4.) and metallisation (5.). A generation window from 64kbit to 64Mbit density is chosen. Optical lithography exploiting deep UV wavelength in conjunction with advanced resist schemes is likely to suffice even for the 64M generation with 0.3 to 0.4 µm minimum features (Fig. 1). 3D cells became standard in the 4M generation, many refined versions have been published. Vertical cell transistors may come into practical use in the 64M generation earliest. The pathway of V_{CC}-reduction is quite clear in view of the 3.3 V JEDEC proposal for the 64M[1]. Progress in patterning technology is exemplified by the cell size reduction (Fig. 2) by a factor of 2.7 per generation in the average. The one transistor cell charge however remains fairly constant since sense amplifier noise margins and reliability forbid scaling.

2. DRAM CELL STRUCTURES

The one transistor DRAM cell consists of a storage capacitor and the transfer transistor isolating the capacitor from the bitline (BL). Up to 1M a planar MOS capacitor was used. For the 3D cells in the 4M generation, the two main approaches are the trench cell with the capacitor formed within a trench in the substrate and the stacked cell where the capacitor is formed as a polysilicon / dielectric / polysilicon stack on top of the transfer transistor[2) 3)]. Since that time a large number of different 3D cells has been proposed (Fig. 3). This cell evolutionary tree shows two main branches, the trench type and the stacked type. For trench type 16M cells the trench-trench leakage problem has to be solved. Two approaches to are to use the substrate as capacitor plate (Inverted Trench Cell), or to minimize the depth of the trench doping. Relaxation of the trench aspect ratio is achieved in Surrounding Trench Cells where the trench serves as part of the cell isolation. The basic problem for the stacked cell is its limited cell capacitance. To increase capacitor area either

the vertical portions are increased or mulitlayered structures are used.

Examples of the evolution from 4M to 64M are shown in Table 1[4)5) 6) 7)] . The aspect ratio of the trench has to be increased from 4 to 11 together with reducing the effective dielectric thickness from 12 to 5 nm.

Some approaches for arranging the transfer transistor vertically are shown in Fig. 4. These concepts need very deep trenches and a well controlled electrode etchback. The capacitor node contact has to be formed in the trench.

Trench Cell				Stacked Cell			
	4M	16M	64M		4M	16M	64M
Cell Structure	Trench	Stacked Tr.	Oxide Isol. Stacked Tr.	Cell Structure	Stacked	Dash	Fin Stacked (2 Fin)
Trench Depth (µm) Cross Section (µm²)	4.0 0.9x1.0	4.5 0.7x0.95	5.5 0.5x0.7	Stack Height (µm)	0.6	0.9	1.1
Effect. Dielectr. Thickness (nm)	12	9	5	Effect. Dielectr. Thickness (nm)	7	5	4
Cell Capacitance (fF)	35	35	35	Cell Capacitance (fF)	35	35	27
Innovations:	Trench Etching, Trench Doping, ONO Dielectric	Shallow Trench Doping, Interpoly Dielectric	Selfaligned Trench Sidewall Contact	Innovations:	Stack Contact, Interpoly Dielectric	Double Self Aligned Stack Contact	Fin Formation

Tab. 1 Technology Features for Trench and Stacked Cells

3. CAPACITOR DIELECTRIC

In order to compensate for shrinking lateral capacitor dimensions, the SiO_2 thickness has been reduced substantially until 1M (8 - 10 nm). In 3D cells multilayer dielectrics, preferrably ONO, became a necessity. Reducing the ONO thickness d_{eff} to 5 nm, a 64M cell with 30 fF is feasible[8) 9)]. The capacitor dielectric area per chip dramatically increases for 3D cells up to 400 - 500 mm² for 64M (Fig. 5). The data are derived from cell studies using stacked trench (16M) and oxide isolated stacked trench (64M). The E-field on the capacitor dielectric has been and will be kept below 3 MV/cm under nominal conditions (Fig.6). The major factors are $V_{CC}/2$-plate voltage, 3D cells and array voltage reduction from 16M onwards. ONO layers will probably reach their limit in the 64M generation. Investigations of d_{eff} = 5nm structures indicate sufficient reliability[9)], but the onset of direct tunneling strongly increases leakage currents for d < 5 nm. Alternatives are high ϵ dielectrics. Considerable progress has been achieved with Ta_2O_5[10)]. Also investigations of ferroelectric materials such as PZT has started for DRAM applications[11)]. A high charge storage density of around 7µCb cm^{-2} has been found.

4. SELF ALIGNED TECHNOLOGIES FOR DRAM CELLS

With edge overlay accuracy resisting scaling, selfaligning technologies became necessary. The various approaches for selfaligned bitline contact (BLC) and cell node contact (CNC) are summarised in Tabe 2[4) 12)]. All these technologies use an oxide or nitride encapsulation of the wordlines (WL) either by a selective oxidation or a spacer technique. The complexity of BLC or CNC depends on the requirements for the thickness of the intermediate oxide between WL and BL. If the WL encapsulation gives a sufficient low coupling capacitance, selfalignment is very simple. The contact mask can overlap the gate without any further precautions. If the WL encapsulation is not sufficient for WL to BL isolation either with respect to planarization or with respect to coupling capacitance, more sophisticated techniques have to be used. The most common approach is to use an etchstop layer on top of the WL encapsulation as shown in Fig.7.

Cell Type	Selfalign. Contact	Technology	DRAM Generat
Trench Transistor Cell with Self-aligned Contact TSAC (NEC, 1986)	BLC	- Nitride Oxidation Barrier on Poly 1 Plate and S/D Regions - Selective Oxide Encapsulation (OE) of Wordlines	4M
Trench Transistor Cell (TI, 1986)	CNC	- Selfaligned Trench Sidewall Contact Opening and Outdiffusion from Poly-Si Storage Node	4M
Fully Overlapping Bitline Contact FOBIC (Siemens, 1987)	BLC	- OE of Transfergate and Etchstop Layer for BL-Contact Opening	4M
Quadruple STC (Hitachi, 1987)	BLC	- OE of Transfergate and Poly-Si "Landing" Pads Overlapping Gate and Fieldoxide	4M
Sheath Plate Capacitor Cell (Hitachi, 1988)	BLC CNC	- OE of Transfergate and Poly-Si "Landing" Pads Overlapping Gate and Fieldoxide - Trench Sidewall Contact Opening and Out-diffusion from Poly-Si Storage Node	16M
DASH Cell (Hitachi, 1988)	BLC, CNC	- Oxide Encapsulation of Wordlines and Bitlines	16M
Spread Source/Drain Transfergate (Toshiba, 1989)	BLC, CNC	- Selective Lateral Silicon Overgrowth of Source/Drain Regions	64M
Oxide Isolated Stack Trench Cell (Siemens, 1990)	BLC CNC	- OE of Transfergate and Oxidable Poly-Si etch stop Layer - Selfaligned Trench Sidewall Opening and Out-diffusion from Poly-Si Storage Node	64M

Tab.2 Self Aligned DRAM Cell Contact Technologies

5. METALLISATION

Conventional AlSi metallisation has already been improved by migration reducing additions such as Cu and barrier layers such us TiN or TiW in present DRAM generations. For a 64M device the total metal length per chip will be around 100 meters. Improved planarisation underneath metallisation will be a necessity. In view of the problems listed in Table 3, Al metallisation still has further improvement potential[13] such as multisandwich structures AlSi/Ti/AlSi[14]. Alternative materials like W are already used by some manufactures for its high electromigration resistance and easy patternability, however with the drawback of a higher sheet resistivity. The most widely investigated and promising approach to relax the contact/via problem are refill techniques, either by deposition/ etchback or by a selective deposition. However apart from its rather sophisticated process features the significant additional process cost seems to postpone practical application to the point of absolute necessity.

INTERCONNECT

problems: electro-, stress migration, hillocks, resistivity

possible solutions:

- AlSi with additions of Cu, Ti, Pd, C
- layered structures: underlying barrier layers (e.g. TiN, TiW)
  multisandwich (e.g. AlSi/Ti/AlSi)
  W encapsulation of Al
- alternative metals: W, Cu

CONTACTS / VIAS

problems: contact resistance, metal-silicon and metal-metal interaction, step coverage/ reliability, topography for subsequent processes

possible solutions:

- refill by CVD deposition & etchback (W, Poly-Si)
- refill by selective CVD (W, Al, Pd, Ni, Mo, Cu, WSi_2, Si, Ge)
- refill by bias sputtering
- laser reflow of sputtered Al
- electroless deposition: Co, Ni, Pd
- pillar technique

Table 3 Problems and innovative approaches in metallisation

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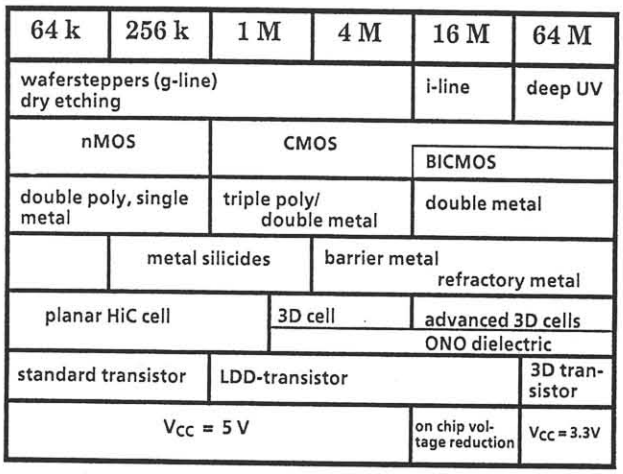

Fig.1 Major innovations in DRAM technology from 64k to 64M. In reality transitions occur smoother then drawn for reasons of simplicity.

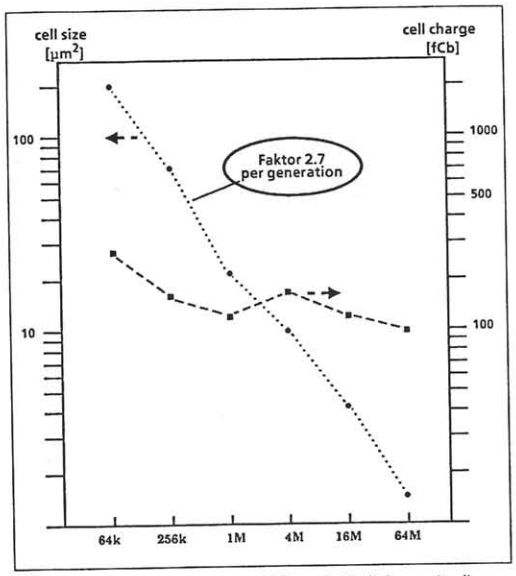

Fig. 2 Evolution of one transistor cell size and of cell charge. A cell capacitance of 30 fF is assumed for 64M

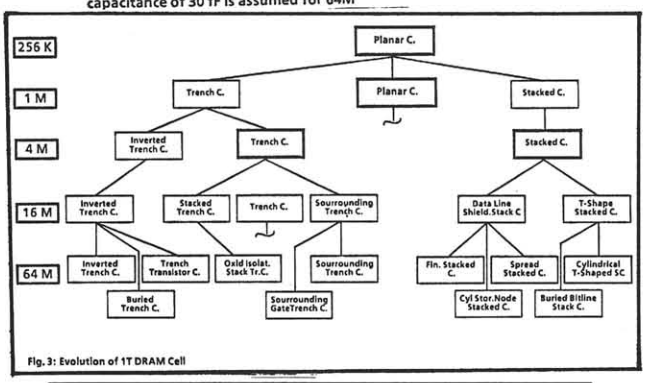

Fig. 3: Evolution of 1T DRAM Cell

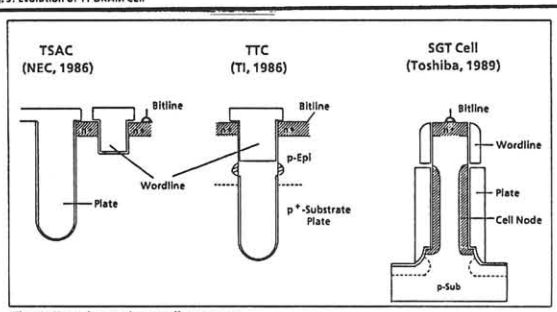

Fig. 4 Trench transistor cell concepts

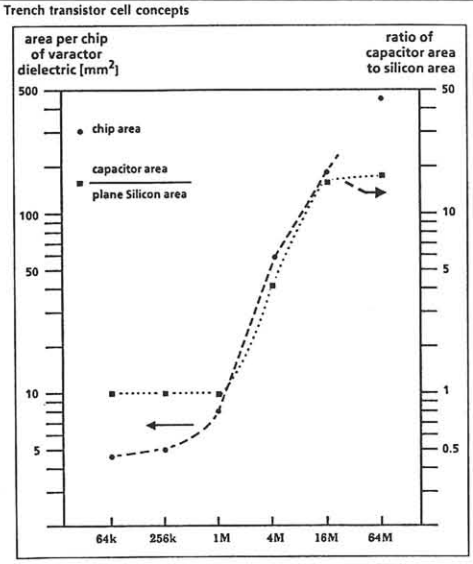

Fig. 5 Increase of area of varactor dielectric per chip and area ratio ("folding efficiency") from 64k to 64M.

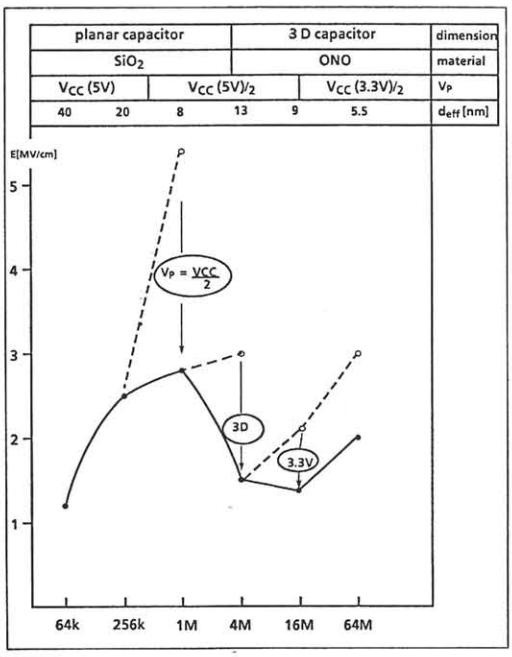

Fig. 6 Electric field exerted on capacitor dielectric. The measures to keep the field well below 3 MV/cm are indicated.

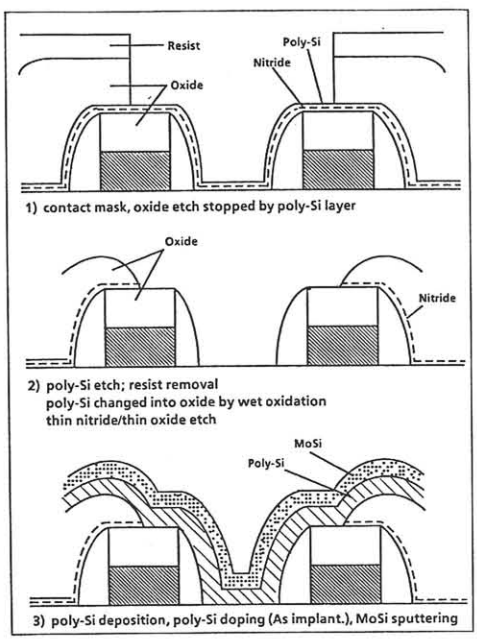

Fig. 7 Process flow for selfaligned bitline contact formation using an oxidable etchstopp layer[5]