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A Stacked Capacitor Cell with Ring Structure

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A novel stacked capacitor cell with a ring structure is proposed. In this structure, storage capacitance is doubled by adding the ring electrode around the main electrode. Since this ring electrode is self-aligned, no additional photolithography step is necessary. This also permits the minimized spacing between capacitors beyond the resolution limit of photolithography and a larger margin for storage electrode alignment to the contact hole. No explicit degradation in electrical characteristics by the addition of the ring electrode is observed. Relatively low electrode height of 500 nm is enough to achieve a capacitance of 30 fF for a 0.8 μm^2-cell. The Ring Capacitor has excellent properties which make it an attractive candidate for the 64M and 256Mbit DRAMs.

1. Introduction

Reduction of cell capacitance resulting from the decrease in memory cell area is one of the most serious obstacles that limit further integration of DRAMs. For the 64 Mbit DRAM with the memory cell area of around 1.5 μm^2, it is difficult to obtain enough capacitance even with a material of large dielectric constant like TaO_x, if the conventional stacked capacitor structure is used. This capacitance problem becomes more critical for lower voltage operation. Therefore, many three-dimensional sturctures have been proposed in order to realize a large enough capacitance, which include double stack (1), fin (2), cylindrical electrode (3), and box structures (4).

Here, a novel stacked cell capacitor having a ring structure is proposed. With this structure, it is possible to obtain sufficient capacitance for the 64 Mbit DRAM and beyond without additional photolithography step.

2. Characteristics of the Ring Capacitor

In the new stacked cell capacitor structure, an additional electrode with the shape of a ring is added around the conventional stacked electrode. The total area of the storage electrode is increased by taking advantage of both sides of the ring without increasing the cell area. Fabrication procedure of the ring capacitor, shown schematically in Fig. 1, is as follows:

(a) Deposition of SiO_2 and Si_3N_4 layers and contact hole formation.

(b) Deposition of poly-Si and SiO_2 and patterning of SiO_2 for poly-Si etch mask.

(c) Poly-Si etching, leaving thin poly-Si layer.

(d) Deposition and etch-back of SiO_2 for oxide sidewall formation.

(e) Deposition and etch-back of poly-Si to form a poly-Si sidewall, which will be used as a ring electrode.

(f) SiO_2 sidewall removed by wet etching with buffered HF using the Si_3N_4 layer as an etch stop. N^+ doping of the storage node.

(g) Formation of the capacitor dielectric film, thermally oxidized LPCVD Si_3N_4, and deposition of cell plate poly-Si.

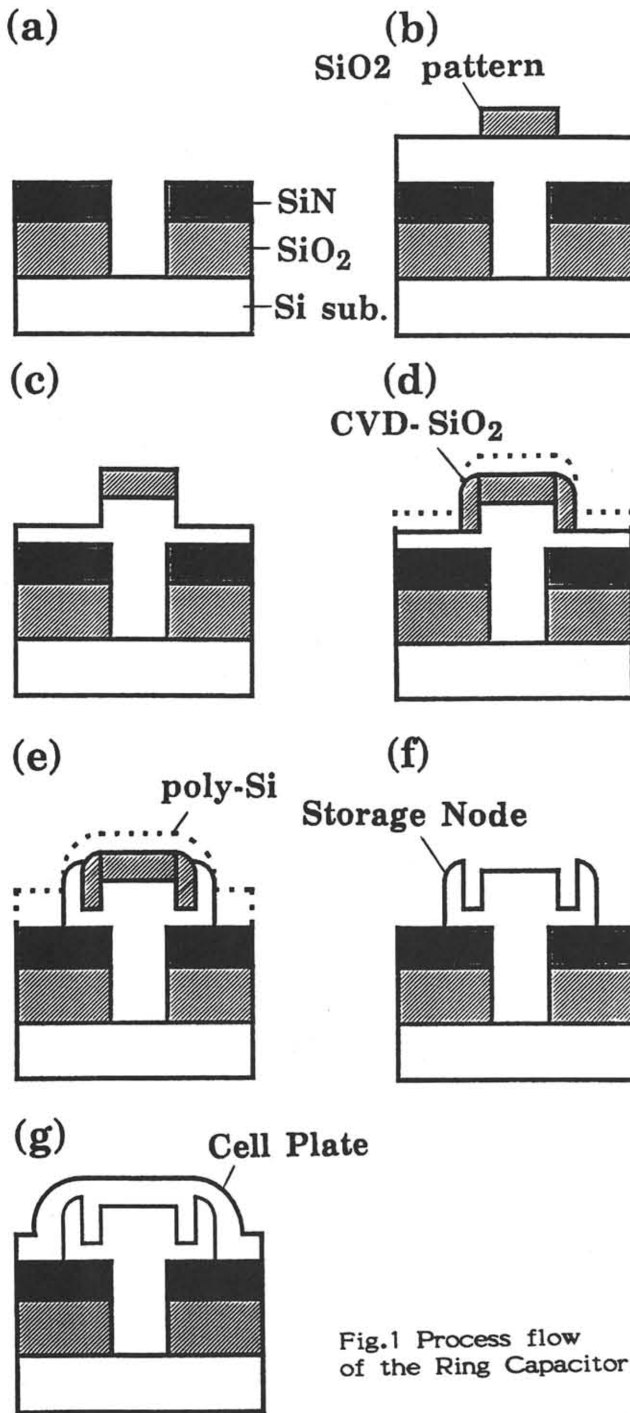

Fig.1 Process flow of the Ring Capacitor

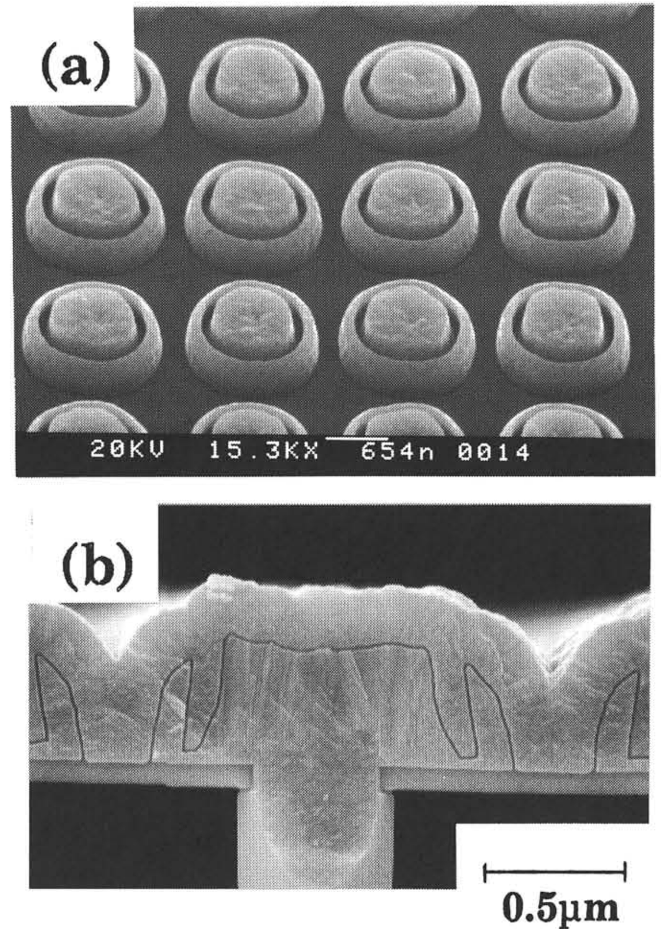

Fig.2 SEM micrographs of the Ring Capacitor
(a) bird's eye-view of storage electrodes
(b) cross-sectional view after deposition of the plate electrode.

Since the ring electrode is self-aligned around the main electrode, no additional photolithography step is necessary. The distance between neighboring capacitors can be reduced to less than the resolution of photolithography, thus enabling effective use of the cell area. Moreover, the enlargement of storage electrode also permits a larger margin for storage electrode alignment to the contact hole.

The SEM picture of ring capacitors are shown in Fig. 2-(a). One notes that it is possible to form a thin ring electrode with a width of about 0.1 μm around the central electrode of 1 μm diameter, with the gap between the ring and the main electrodes of about 0.1 μm. It is thus feasible to achieve a 0.25 μm spacing between neighboring capacitors, which is well below the current resolution limit of photolithography. The cross sectional SEM picture of the electrode in Fig. 2-(b) shows that capacitor dielectric and cell plate poly-Si completely fill the valley between the central and the ring electrodes, which suggests that LPCVD processes for silicon nitride and poly-Si have good enough coverage.

3. Electrical Characteristics

For the electrical characterization, storage capacitors with a composite layer of SiO_2/Si_3N_4(ON) having the equivalent oxide thickness of 6.1 nm were fabricated. The geometry of the ring structure was designed so as to increase the storage area by a factor of about two. Measurement was done using 1.4 million capacitors with 6.8 μm^2 cell size connected in parallel. High frequency C-V characteristics in Fig. 3 shows capacitance of 26.2 fF/cell for the stacked capacitor without a ring. Adding the ring electrode almost doubles the capacitance to 52.3 fF/cell, which agrees well with the increase in the storage area. In the case of positive bias, decrease of the capacitance due to depletion of the plate electrode is only by a few percents, which suggests that impurity diffusion for doping the electrode down to the deepest part of the valley of the ring capacitor poses no problem.

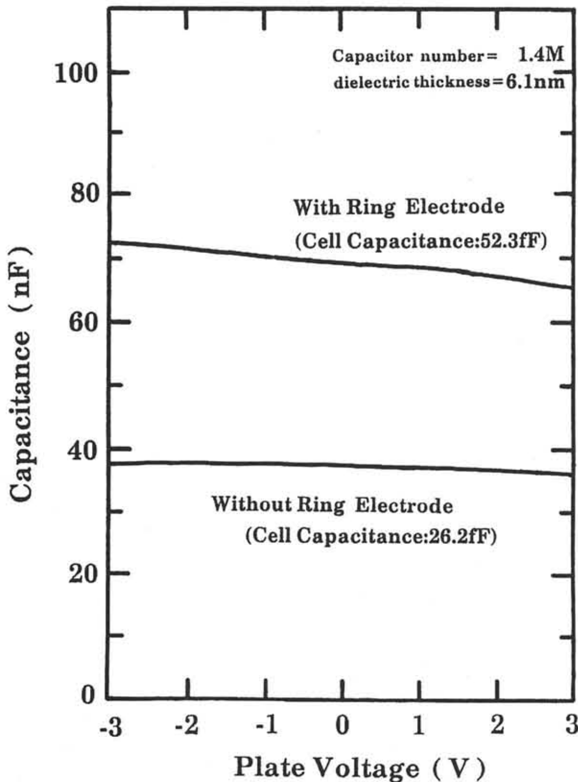

Fig.3 C-V characteristics of capacitors with and without Ring electrode. Capacitance is measured for 1.4 million capacitors with 6.1 nm thick dielectric film.

Figure 4 shows I-V characteristics of the capacitors. At negative bias, the leakage current of the ring capacitor only increases to an extent which corresponds to the increase in the storage area. Leakage current per cell of the ring structure is well within the allowable limit of 5 fA/cell. On the other hand, when positive bias is applied, the ring structure shows higher leakage current than the structure without a ring due to concentration of electric field at the ring. However, this is not a serious problem because lifetime of the ON dielectric layer is determined by negative bias which causes larger leakage current than positive bias.

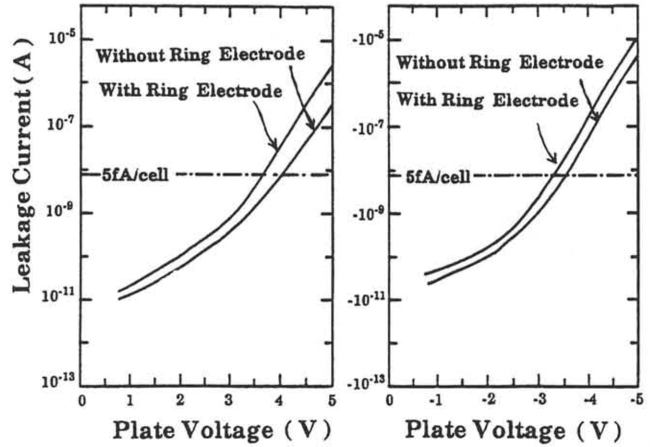

Fig.4 I-V characteristics of capacitors with and without Ring electrode. Leakage current is measured for 1.4 million capacitors with 6.1 nm thick dielectric film.

Distributions of breakdown voltages of the capacitors for the critical current density of 0.2 $\mu A/cm^2$ are shown in Fig. 5. Ring capacitors have the same distribution as those without rings and show no defects at low electric field. Figure 6 shows time dependent dielectric breakdown characteristics of ring capacitors at high field stress. No degradation of the lifetime due to the addition of ring electrodes was observed. The estimated storage capacitance of the ring capacitor with electrode height of 500 nm and dielectric thickness of 5 nm is shown in Fig. 7, where the capacitor-over-bitline

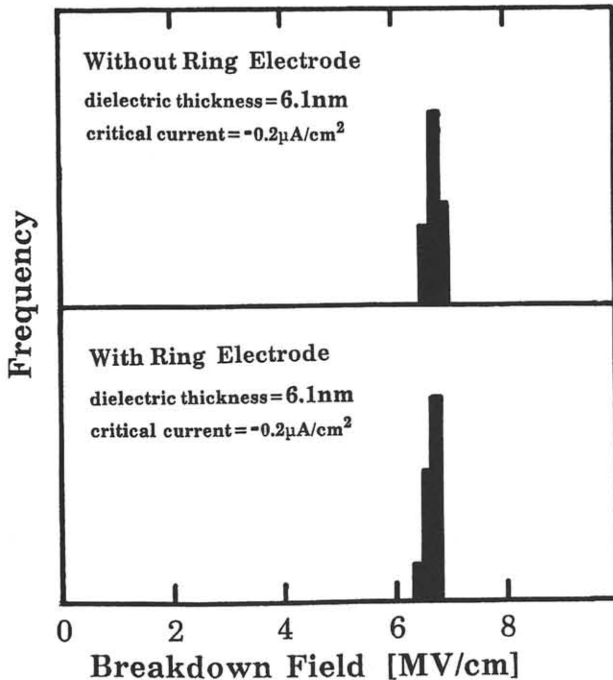

Fig.5 Breakdown-field distribution of capacitors with and without Ring electrode. Field is reduced to oxide and critical current density is $0.2\mu A/\mu m^2$.

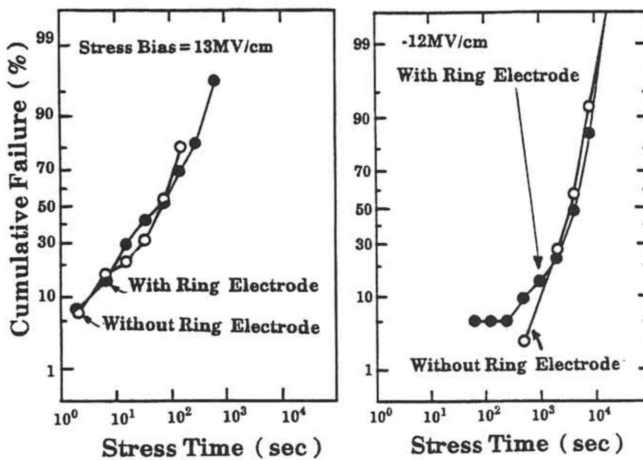

Fig.6 Comparison of TDDB characterisics between conventional and Ring Capacitors.

structure [2] [5] is assumed. It was also assumed that both the spacing between the central and the ring electrodes and the ring electrode thickness are $\sqrt{(S/2)}/10$, where S is the memory cell area. Since a ring capacitor is expected to store three times the charge of a conventional stacked capacitor without difficulty, a capacitance of 30 fF can be obtained from the cell area of 0.8 μm^2, with a relatively low electrode height of 500 nm.

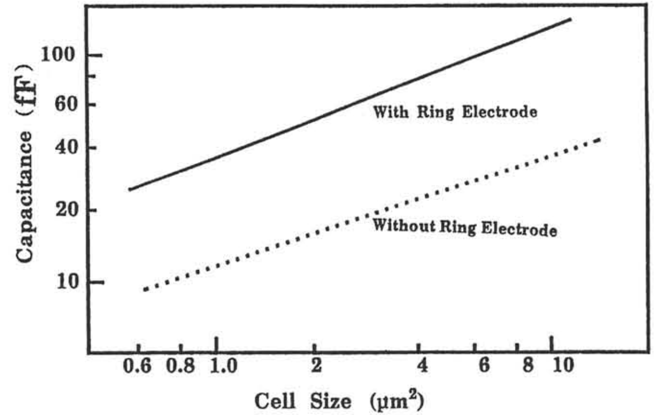

Fig.7 Calculated capacitance of the Ring Capacitor. It is assumed that the storage electrode height is 500nm, the dielectric film thickness is 5nm, the main electrode spacing is $6 \cdot \sqrt{(S/2)}/10$, and both the ring-main electrode spacing and the electrode thickness are $\sqrt{(S/2)}/10$, where S is the cell area.

4. Conclusion

A novel stacked cell capacitor with a ring structure has been proposed. It has been found that twice the capacitance of the conventional stacked cell capacitors can be obtained. From the measurement of leakage current, break down voltage, and TDDB characteristics, it has been confirmed that there is no degradation in these electric properties by the addition of ring electrodes. Therefore, the stacked cell capacitor with a ring structure has excellent properties which make it a promising candidate for the 64 M and 256 Mbit DRAMs.

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REFERENCES

1)T.Kisu et al.,Ext. Abs. 20th SSDM,p.581(1988)
2)T.Ema et al.,IEDM Tech. Dig.,p.592(1988)
3)W.Wakamiya et al.,Symp. VLSI Tech.,p.69(1989)
4)S.Inoue et al.,Ext. Abs. 21th SSDM,p.141(1989)
5)S.Kimura et al.,IEDM Tech. Dig.,p.596(1988)