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A 64MBit Stacked-Trench-Capacitor Cell

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Implementation of very thin capacitor electrodes and of a new multilayer dielectric has been realized in a Stacked-Trench-Capacitor Cell with 64Mbit-DRAM feature sizes. Cell capacitances in the range of 35fF are obtained at a trench depth of 5μm. The cell exhibits a relatively flat topology and good device characteristics like low leakage currents and α-particle sensitivity due to the electrical isolation of the capacitor from the substrate. Key features of the technology, device parameters, and memory array performance will be discussed.

1. INTRODUCTION

VLSI-DRAMs rely on cell approaches that enlarge the effective area of the storage capacitor at small cell sizes. A variety of cells are known which are modifications of basically two main concepts, the Trench-Capacitor-Cell and the Stacked- Capacitor-Cell. The former, being electrically similar to a planar cell, was established as a widely used concept in 4Mbit products. The latter seems to gain more attention in the 16 and 64Mbit generation, especially with enhancements like fin[1)2)] or cylinder[3)] structures.

We have been comparing the two basic approaches since the 4Mbit generation[4)] and have now investigated on the 64Mbit level a merged concept combining the advantage of trench i.e. good planarity and large area with the superior electrical behavior of the stacked capacitor. It will be shown that a capacitor in a trench featuring two poly-Si electrodes which are isolated from the substrate is very well suited to meet 64Mbit requirements. This cell type is highly compatible with our 16Mbit-DRAM approach.

2. SPECIFICATIONS AND TECHNOLOGY

Specifications of the experimental 64Mbit-DRAM are summarized in Table1 followed by a brief description of the process.

Memory cell arrays with a slightly increased word and bitline pitch (1.0/1.1μm) were processed for electrical characterization using g-line lithography, Na = 0.55, and high contrast resist. The size of the trench (0.6*0.5μm) corresponds to the final 64Mbit cell. The cell is located in a 2μm deep p-well with a doping concentration of 2E17cm^{-3} at the surface. Compared to our 16Mbit-process[5)] shallow trench isolation, $TiSi_2$-bitline with self aligned contacts, and STT capacitor formation is introduced. The key steps for the capacitor fabrication are: after trench side wall is oxidized, the oxide at the contact region is removed isotropically and self aligned to the trench corner at a depth of 0.5μm with a contact mask. This is followed by CVD-poly-Si deposition for the storage node, anisotropic etch back, capacitor dielectric growth, and poly Si deposition for the cell plate.

Technology	0.4μm 2Al twin-well CMOS p-sub 2Ωcm 2poly Si, $TiSi_2$-Bl, poly-Si/Al-Wl
Cell	Stacked Trench 0.9*1.8 = 1.62μm^2 35fF(typical) Vcc/2 cell plate
Transistor	Ln,Lp = 0.4μm tox = 10nm
Access time	40ns
Power supply	3.3V (Vbb = -1V internal)
Chip size	9.3*19.7 = 183mm^2

Table 1. Target parameters of 64Mbit-DRAM

3. STT-CELL

3.1 Punch through and leakage currents

Due to the isolation of the capacitor electrodes from the substrate, see Fig.1, punch through between neighbouring cells can only occur at the trench contact to neighbouring bit-lines or trench contacts where the isolation oxide was removed. 2D-simulations show that this distance can become as small as 0.25μm using shallow trench isolation with a depth of 0.8μm providing an alignment tolerance of 0.2μm. Due to the small sensitive area of the cell generation currents are in the range of 0.1pA/cell at 3.3V bitline voltage. A charge transfer of 25fC has been estimated using an analytical model to account for the α-particle sensitivity of the cell node at the given geometry and doping concentrations. Gated diode or band to band tunneling currents do not appear in this cell type.

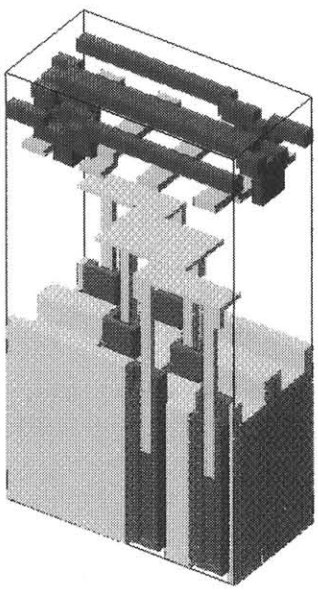

Fig.1 3D-view of 64Mbit-STT cell

3.2 Capacitor area

One of the key problems of the STT cell with a 0.6*0.5μm designed trench hole is the reduction of the effective capacitor area by tapered trench profiles, trench sidewall oxide, and storage node electrode.

Fig.2 shows a cross section of the improved 64M-capacitor. Trench etching was performed using commercially available equipment (Applied Materials P5000E). A unique process with HBr chemistry in magnetically enhanced plasma was developed to etch 5μm deep trenches with almost vertical side walls and rounded bottom. The thickness of the trench side wall oxide is reduced to 40nm. When a "1" is stored on the storage node the trench is surrounded by a space charge layer, however, thermally generated electrons can not reach the storage node due to the high doping concentration of the p-well (2E17cm^{-3}).

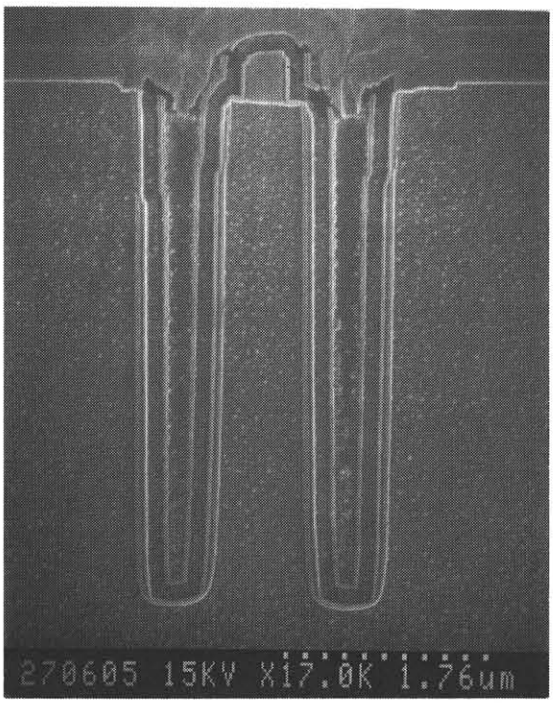

Fig.2 Cross section of the capacitor after poly-Si deposition

For the thin capacitor electrodes we used a deposition of amorphous Si with in situ As doping which allows to adjust the doping concentration. First a 5nm thick highly As doped Si layer is deposited followed by undoped Si deposition. After annealing the doping concentration in the 40nm thick layer is in the range of (3-5)E19cm^{-3}, see Fig.3. This concentration minimizes the depletion layers in the electrodes and on the other hand allows the controlled growth of the capacitor dielectric with low defect density. The sheet resistance of this very thin electrode is below 5kΩ/□. The RC-time constant of the capacitor is negligibly small for write and read cycles in the range of nanoseconds. The same technique was used for the cell plate with a thickness of 150nm.

3.2 Dielectric

An oxide-nitride-oxide (ONO) multilayer dielectric was used for the 64Mbit concept. The ONO-layers were composed of a 2nm thermal bottom oxide, a 4nm LPCVD nitride, and a 1.5nm thermal top oxide (dry oxidation with HCl). The

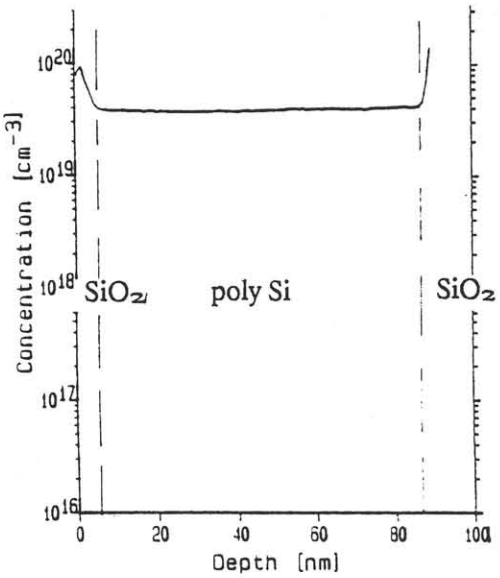

Fig.3 As doping concentration of in situ doped electrodes

thicknesses of the bottom oxide and the nitride layer were determined by ellipsometry and the top oxide thickness by ellipsometry and CV-measurements of the complete ONO-layer. The IV-characteristic of the multilayer dielectric for both gate polarities is shown in Fig.4. For electric fields below 5MV/cm the IV-curves of the ONO-layers are always above a Fowler-Nordheim-characteristic calculated with the data of a silicon-oxide-polysilicon structure. The higher leakage currents of this thin multilayer are due to direct tunneling processes in the extremely thin oxide layers. The breakdown distributions of the ONO-dielectric were evaluated in constant voltage tests. The defect density was below 0.2cm^{-2}. More details about the 5nm ONO-dielectric are published elsewhere [6].

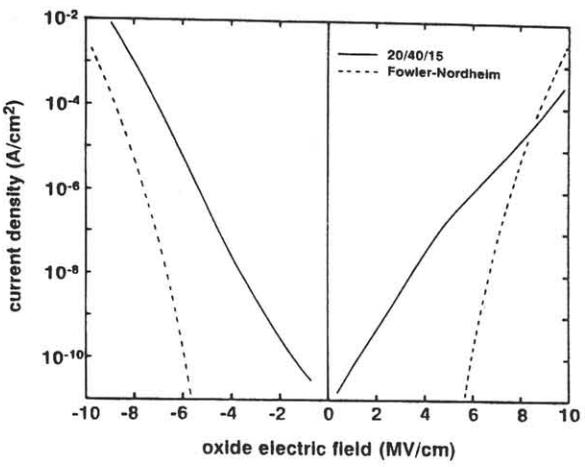

Fig.4 IV-curve of the ONO-dielectric (layer thicknesses in Å).

3.3 Cell capacitance

With the doping concentration of 3E19cm^{-3} for both capacitor electrodes and the new multilayer dielectric an average specific capacitance of 5.5fF/μm^2 is obtained at bias conditions from +1.65V to -1.65V taking into account the two space charge layers in the electrodes. STT cell capacitances in the range of 35fF are achieved with a trench depth of 5μm as shown in Fig.5. The reduction of the capacitor perimeter for the 40nm sidewall oxide und 40nm electrode is only 0.5μm which is 25% of the initial perimeter. For comparison, capacitors with 16Mbit geometry (1.0*0.7μm) and more conventional layer thicknesses of 70nm side wall oxide, 150nm electrode, and 10nm dielectric provided a cell capacitance of 20-25fF. In this case the reduction of the capacitor perimeter amounts to 1.5μm which is in the same range as the total 64Mbit-capacitor perimeter.

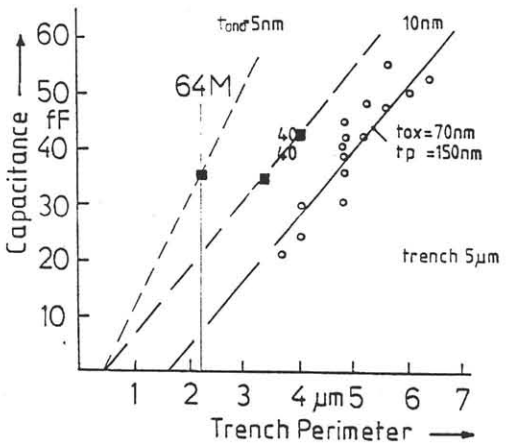

Fig.5 Cell capacitance as a function of designed trench perimeter for different thicknesses of poly-Si and dielectric

3.4 Transistor

The cell transistor as well as the periphery transistors were optimized allowing for a minimum channel length of 0.3μm. Due to the thin gate oxide the body effect of the cell transistor is relatively small, see Fig.6. With Vbb = 1.5V + 3.3V threshold voltage remains below 1.3V which limits the wordline boost to read/write the full signal in/out of the cell to below 5V. With 94mV/decade the subthreshold current at 4V and 90C is about 0.1pA/cell.

Gate delay of periphery transistors characterized with loaded (1pF, W = 10μm) and unloaded inverters is 750ps and 70ps, respectively. Compared to 16M transistors at 5V, delay times for 3.3V operation are improved by 30%.

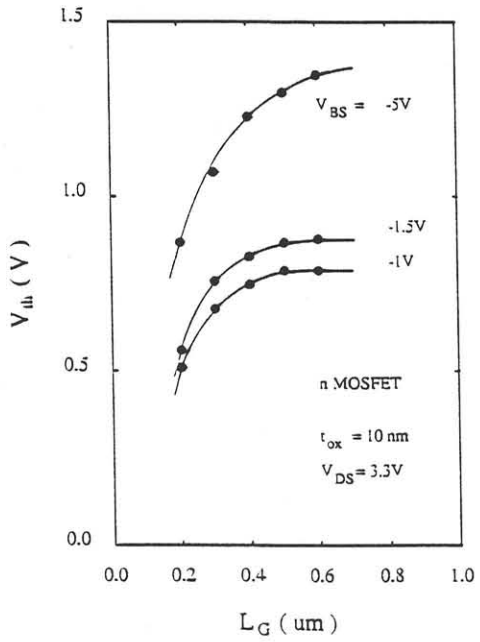

Fig.6 Threshold voltage of cell transistor for different substrate bias voltages

3.5 Cell performance

With the 3D-simulated bitline capacitance of 0.9fF/cell, see Fig 6, which is in good agreement with measured values at larger bitline pitches, the cell signal is in the range of 160mV for 256 cells per bitline at a minimum bitline voltage of 3V. This provides sufficient noise margins of 25fC for α-particles, as well as for coupling effects and process tolerances.

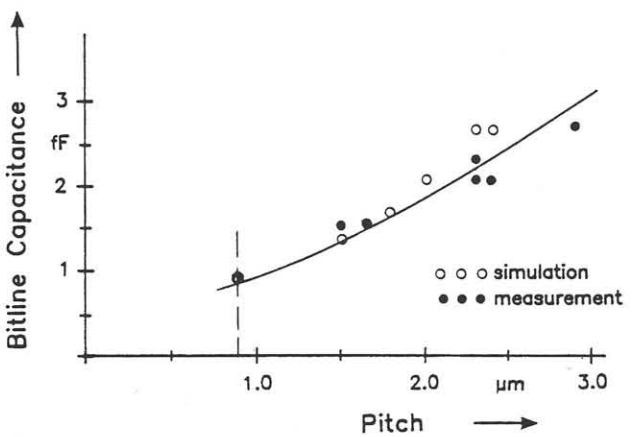

Fig.7 Measured and simulated bitline capacitances

A further feature of our cell concept is the shunted wordline. The Al line with a total length of 2048 bitline pitches is contacted 8 times to the poly word line providing a RC time constant of 1ns as can be seen from Fig.8. The short rise time of the wordline is considered as an important advantage over 3D-STC concepts, which are expected to use single polycide wordlines because of the nonplanarity of their storage nodes. Thus the memory can be segmented in 128*512K subarrays with only two row decoders and wordline drivers, 32 sense amplifiers, and 1 column decoder in the middle of the chip. The result is a chip size of 183mm² with a very high cell to chip ratio of 57%.

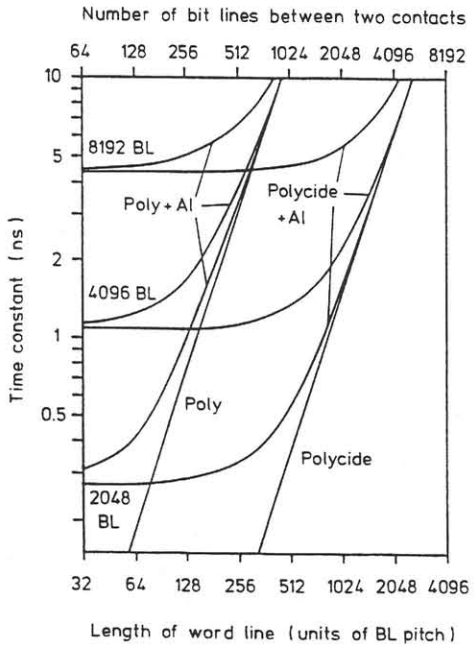

Fig.8 Time constant of poly, polycide, and with Al shunted wordlines

4. CONCLUSIONS

A 64Mbit STT-cell with a cell size of 1.62μm² and an effective capacitor diameter of 0.4μm yields capacitances of 35fF. The application of extremely thin capacitor electrodes combined with 5nm dielectric has been successfully demonstrated. The low parasitic bitline capacitances together with the low resistivity wordline of our Stacked-Trench-Capacitor Cell result in a small chip size due to the segmentation in large sub-memory blocks with a smaller amount of pitch circuits.

5. References

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