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# Fabrication of Storage Capacitance-Enhanced Capacitors with a Rough Electrode

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In order to produce high performance capacitors with a rough surface polysilicon film as a storage electrode, we investigate various fabrication conditions for polysilicon films. We fabricated such capacitors that attained 1.5 times as much capacitance as those with a conventional polysilicon electrode and essentially the same current voltage characteristics. In the evaluation of their reliability, we found that they are sufficient for next generation DRAM applications.

#### 1.Introduction

A storage capacitor consisting of a thin dielectric film in between polysilicon film layers is a key element of stacked type mega bit DRAMs. Keeping storage capacitance on a limited cell area is one of the crucial issues for fabrication of the storage capacitors. For this purpose, effectively thinner dielectric films such as Ta<sub>2</sub>O<sub>5</sub><sup>(1)</sup> are used. We may also enhance the surface area of the storage electrode by adopting three dimensional structures such as cylindrical capacitors (2). As another method of enlarging the area, a technology of engraving storage electrode polysilicon film covered with a resist/SOG mixture was proposed<sup>(3)</sup>.

It has been found that the polysilicon surface formed by the low pressure chemical vapor deposition (LPCVD) method becomes quite rough at certain deposition conditions  $^{(4)}$ . Using this method, we fabricated stacked capacitors with a storage electrode deposited under such deposition conditions and evaluated their electric characteristics.

### 2.Experimentation

Polysilicon films were deposited on thermally grown oxide films by the LPCVD method using both SiH<sub>4</sub> and nitrogen or SiH<sub>4</sub> alone at deposition temperature, Td, ranging from 540°C to 640°C. Figures 1-(a)~(b) show SEM micrographs of the polysilicon film deposited at 560°C, 580°C and 600°C, respectively. Polysilicon film deposited at 580°C shows quite a rough surface consisting of about 100 nm high bumps.

We also observed this phenomenon in the case of the polysilicon film deposition on CVD oxide films, CVD nitride films and silicon substrates. No drastic change of the surface asperity was observed when the



(a) Td=560°C (b) Td=580°C (c) Td=600°C Fig.1 SEM micrograph of polysilicon film deposited at 560°C, 580°C and 600°C.

polysilicon film was doped or annealed.

Results of a X-ray diffraction pattern of these films are shown in Fig. 2. A+ deposition temperature of 600°C, the (111), (220) and (311) diffraction peaks are observed, while the film exhibit an amorphous state at 560°C. Thus such a rough surface appears in a transition region between amorphous and polycrystalline structure. At the transition temperature, <110> texture diminishes but <311> and <111> texture survive. This observation suggests that the bumps on the polysilicon film consist of grains with <311> and <111> textures which grow from the filmsubstrate interface (5).

The structure of a fabricated stacked capacitor is schematically drawn in Fig. 3. It consists of a  $SiO_2/Si_3N_4$  dielectric film with oxide equivalent thickness of 8 nm, a 200 nm thick upper electrode and the polysilicon storage electrode deposited at temperatures from 570°C to



Fig.2 X-ray difraction pattern of the polysilicon films.



Fig.3 Schematic drawing of the structure of fabricated stacked capacitor.

640°C. The thickness of the storage electrode was set to be 200 nm. The storage electrode polysilicon film was doped by implanting arsenic. The upper electrode was doped by phosphorous diffusion.

# 3.Results and Discussion

Normalized storage capacitance as a function of the deposition temperature is plotted in Fig. 4. When storage electrodes are formed at  $575^{\circ}$ C, the capacitors show 1.55 times as much capacitance as those with conventional polysilicon film electrodes (Td =  $620^{\circ}$ C). Since the same dielectric films are used for all the capacitors, the increase of the storage capacitance is attributed to the enhancement in surface area of the storage electrodes.

Figure 5 depicts the leakage current density vs. oxide equivalent field strength characteristics of capacitors with both the rough surface electrodes (Td =  $575^{\circ}$ C) and the conventional ones. The oxide equivalent field strength,  $E_{ox}$ , is defined by

$$E_{ox} = \frac{V_g}{t_{ox}} , \qquad (1)$$



Fig.4 Normalized capacitance vs. deposition temperature of the storage electrode. Bars denote standard deviation of the storage capacitance within a wafer. where Vg and  $t_{ox}$  denote gate bias voltage and oxide equivalent thickness of the dielectric film, which is 8 nm, respectively. The leakage current density shown in Fig. 5 is taken into account the enhancement of the capacitor surface area. Capacitors with both the rough and the conventional electrode show no significant difference.

Breakdown voltage distributions of the capacitor with our rough and the conventional storage electrode are shown in Fig. The capacitor with our rough storage 6. electrode may appear to have 0.5-1 V lower However, since we breakdown voltage. adopted the same judgment current for both types of capacitors, the figures show breakdown voltages corresponding to different current densities. Although field concentration at the rough electrode surface is expected to be higher than the at the conventional electrode, both one types of the capacitors show essentially the same current-voltage characteristics. This is because the dielectric film of SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub> structure is not so sensitive to the electric field as that of SiO2 layer alone (3).

Figure 7-(a) shows relationships be-

tween time to 10% cumulative failure and applied oxide equivalent electric field obtained by time dependent dielectric breakdown (TDDB) measurement under constant electric field stresses. Capacitors with our rough electrodes have a lifetime about two orders of magnitude shorter than those with the conventional ones under positive base stresses. On the other hand, they do not show significant differences in the case of negative bias stresses. The lifetime of the capacitor with our rough electrode at an operation condition of 3MV/cm is estimated to be longer than 1X10<sup>10</sup> seconds, which is sufficient for DRAM applications. The degradation of TDDB characteristics can be attributed to the field concentration at the top of the bumps or V shaped valley between the bumps on the storage electrode.

In order to take into account the effect of the capacitance enhancement, the time to 10% cumulative failure is shown in Fig. 7-(b) with respect to the effective field,  $E_{eff}$  defined by the following equations



Fig.5 Leakage current density vs. oxide equivalent electric field



Fig.6 Breakdown voltage distribution at judgment current of 1 mA/cm<sup>2</sup>

$$t_{eff} = \frac{\varepsilon_{ox}\varepsilon_0 S}{C}$$
(2)

$$E_{eff} = \frac{V_g}{t_{eff}}, \qquad (3)$$

where C, S,  $\varepsilon_0$ ,  $\varepsilon_{ox}$  are the measured capacitance, the capacitor area, permittivity in vacuum and the dielectric constant of SiO<sub>2</sub>, respectively. Since the enhancement of the capacitance is equivalent to the use of thinner dielectric films, the effective electric field for the capacitors with a rough electrode become higher than those with a conventional one. Samples with our rough electrode show



Fig.7 Time to 10% cumulative failure as a function of Eox (Fig.7-a) and Eeff(Fig.7-b)

longer lifetime than those with the conventional electrode. This indicates that capacitors with our rough electrode and a thicker dielectric film are more reliable than those with a conventional flat storage electrode and a thinner dielectric film.

# 4.Conclusions

We found that the surface of a polysilicon film at deposition temperature of 575°C is covered with lots of bumps. Storage capacitors with our rough storage electrode show about 50% more capacitance than those with a conventional electrode. The leakage current and constant field TDDB characteristics of the capacitors indicate that they are applicable to the next generation DRAMs without thinning the dielectric films. gate Because of the conformal coverage of the polysilicon film, this technology can be used to enhance the capacitance of three dimensional structure capacitor cells.

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## 6.References

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