A New Stacked Capacitor Structure Using Hemispherical-Grain(HSG) Poly-Silicon Electrodes

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A new technology, which makes storage electrode surfaces uneven, is developed for realizing 64Mbit DRAMs. This technology utilizes a Si film, which is deposited by LPCVD at 550°C. The film surface is composed of hemispherical grains (HSG). The surface area of the HSG-Si film is about twice as large as Si films deposited at other temperatures. The specific temperature, 550°C, corresponds to the transition temperature of the film structure, from amorphous to polycrystalline. By applying the HSG-Si film to a storage electrode for a stacked capacitor, twice the capacitance value is obtained. The capacitance increase makes it possible to reduce the DRAM cell area, even after using a relatively thick dielectric film for higher reliability.

I.INTRODUCTION

In the down-scaling of a DRAM cell, a new storage capacitor is required to provide sufficient capacitance in a limited area. One of the approaches to meet this requirement is to increase the surface area of the storage electrode. Several advanced stacked-capacitor structures, such as fin[1] or cylindrical[2] electrode structures, are categorized in this approach. Another example of this approach is a structure which is called engraved storage electrode[3]. This electrode structure is formed by etching its surface using resist particles as masks. Since this structure is related to the electrode surface, it can be combined with other electrode structures such as fin or cylindrical forms. However, in this engraved electrode structure it is difficult to increase the sidewall surface area of the electrode, which is the dominant part of the electrode surface in a very small DRAM cell.

In this paper, a new technology which results in a silicon film with an uneven surface is proposed, in order to greatly increase the storage electrode surface area. The storage electrode for a stacked capacitor, given by this technology, is entirely covered by the uneven surface. Therefore it can increase the storage capacitance value without increasing cell area or storage electrode height. This capacitor electrode has a sufficiently high reliability to be utilized in 64Mbit-DRAMs.

II.EXPERIMENTS

Si films of 250 nm thickness were deposited on SiO_2/Si-substrate structures by LPCVD. Deposition was carried out with He-diluted SiH_4(20%) gas at 1.0 Torr pressure at various temperatures, measured at the outside of the furnace. The surface morphologies of the deposited Si films were observed by scanning electron microscopy (SEM). Reflection high energy electron diffraction (RHEED) was also used to characterize the surface crystallinity.

The surface areas of the deposited Si films were estimated by measuring capacitance values of stacked capacitors, whose electrodes were made of the Si films. The Si-films were doped by thermal phosphorus diffusion. SiO_2/Si_3N_4 double layer films having 10nm SiO_2-equivalent thickness were employed as the capacitor dielectric films.
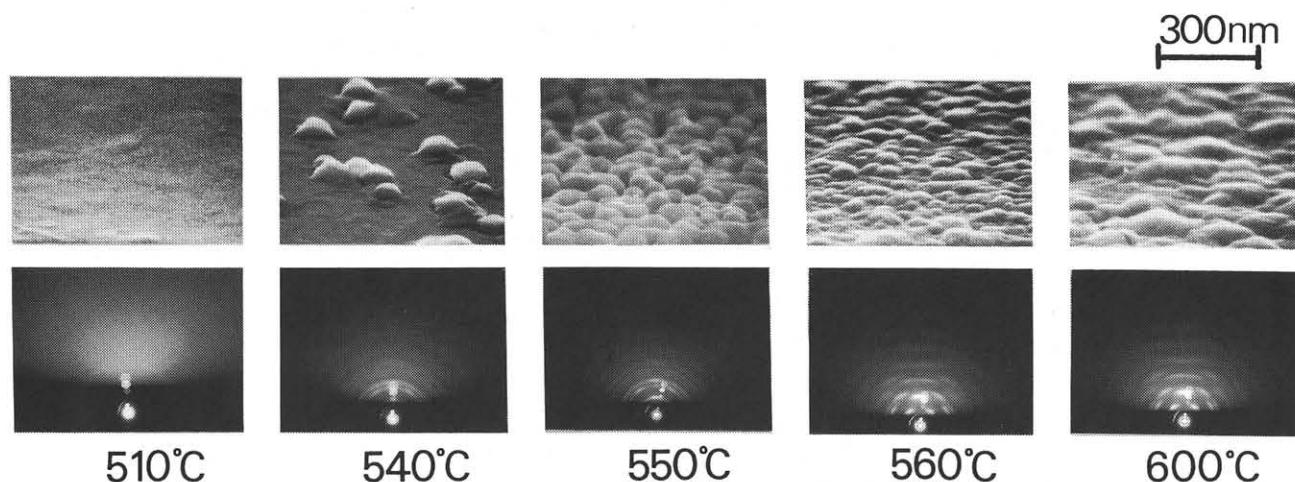
Figure 1   SEM photographs and RHEED patterns of Si surfaces deposited by LPCVD.

The upper electrode was poly-Si deposited by LPCVD at 600°C, followed by thermal phosphorus diffusion.

Another specific stacked capacitor was formed to examine the electric reliability. It was evaluated by measuring electric properties of current-voltage characteristics, breakdown field distributions and time-to-breakdown characteristics.

III. RESULTS AND DISCUSSIONS

Figure 1 shows SEM photographs and RHEED patterns for Si films deposited at 510°C, 540°C, 550°C, 560°C and 600°C. A flat amorphous surface is obtained at 510°C. The surface of the film deposited at 540°C has both amorphous areas and poly-crystalline areas with small grains. The film deposited at 550°C has an uneven surface, which consists of hemispherical-grained Si. This uneven surface film is herein referred to as HSG-Si. The grains on the HSG-Si are approximately 80 nm in diameter. The 560°C and 600°C-deposited films have smoother-grain surfaces than the 550°C-deposited films. Consequently the surface morphology strongly depends on the deposition temperature.

Capacitances of the stacked capacitors are shown in Fig.2 as a function of the deposition temperature. It was found that the capacitance for the stacked Si film, deposited at 550°C, is approximately twice as large as capacitances for
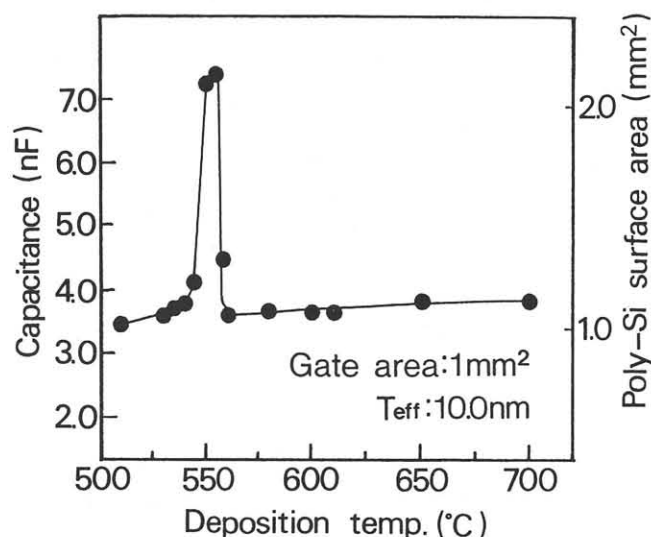

Figure 2   Capacitance dependence on deposition temperature for stacked capacitors.

films deposited at other temperatures. Since the HSG-Si was formed at this temperature, the capacitance increase is attributed to the increase in the electrode surface area. The area enlargement on the 550°C-deposited film corresponds to the fact that the area of the surface, covered with hemispheres, is approximately twice as large as that of the flat surface.

It has been previously reported that the specific temperature, 550°C, is the temperature at which the structure of the Si film, deposited by LPCVD,   changes   from   amorphous   to polycrystalline[4]. This knowledge can explain our surface-morphology variance shown in Fig.1. The

specific surface morphology of the HSG-Si is produced at the transition temperature.

The narrowness of the temperature range in which a larger surface area is obtained, indicated in Fig.2, suggests that severe temperature control is required to deposit uniform HSG-Si films. From this point of view, the stability of the HSG-Si deposition process was examined and then confirmed as follows. The deposition temperature can be well controlled within 5°C, and the surface-area enlargement effect shows excellent reproducibility. The capacitance uniformity is within 2.5% over wafer batches and within 2% over the wafers themselves. Additionally, the surface-area enlargement ratio is almost constant at 2 for HSG-Si films thicker than 100 nm.

Figure 3 shows a cross-sectional SEM view of the 64Mbit-DRAM cell storage electrode, constructed with the HSG-Si. This storage electrode size is 0.86 μm^2 and its height is 0.9 μm. The storage electrode is entirely covered by uneven surfaces. When 600°C-deposited poly-Si film is used for a conventional stacked capacitor, a 5 nm-SiO_2 equivalent-thickness (T_{eff}) dielectric film is required to achieve the capacitance, 30 fF, which is necessary for reliable device operation. On the other hand, the HSG-Si electrode can achieve the same capacitance with a thicker dielectric film: 9.1 nm-T_{eff}. The thicker dielectric film guarantees higher reliability of the capacitor.

Figures 4(a) and 4(b) show I-V characteristics for SiO_2/Si_3N_4 composite films formed on HSG-Si electrodes, in contrast with those on conventional electrodes, shown in Figs.4(c) and 4(d). The T_{eff} thicknesses are noted in Fig.4. The capacitor shown in Fig.4(b) has the same capacitance as that of a conventional capacitor with a 3.5 nm dielectric film. The sizes of storage nodes with which dielectric films store 30 fF are noted in Fig.4. For reliable operation of practical devices, leakage current should be less than 1×10^{-8} A/cm^2 with half of the 3.3 V cell-plate voltage. In the case of the HSG-Si with 6.4
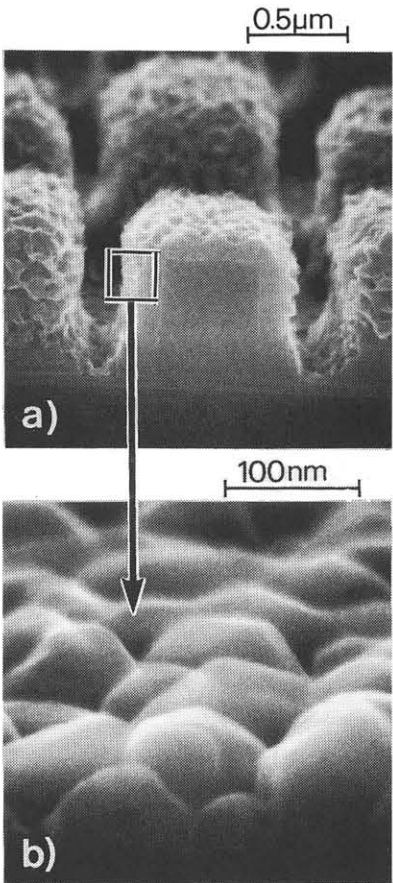

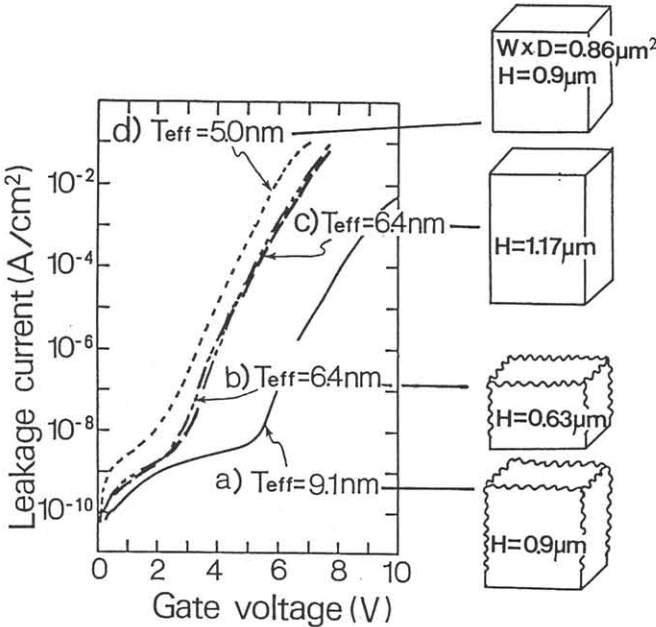Figure 3   64Mbit DRAM storage node SEM photographs.

Figure 4

I-V characteristics of capacitor insulators.
  (a),(b):on HSG-Si electrodes.
  (c),(d):on conventional electrodes.
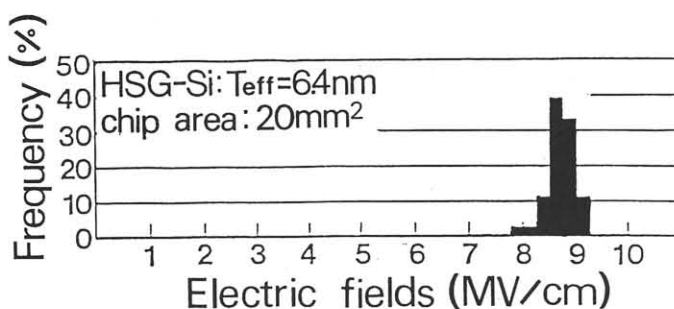Size of storage electrodes, with which dielectric films can store 30fF.

Figure 5

Breakdown field distribution of Teff=6.4nm-SiO_2/Si_3N_4 films on HSG-Si.

Figure 6

Time-to-breakdown of SiO_2/Si_3N_4 dielectric films deposited on HSG-Si electrode and conventional dielectric films.

nm-T_{eff} dielectric film, Fig.4(b), the leakage current is less than 1×10^{-8} A/cm^2 for cell-plate voltages lower than 3 V. This voltage, 3 V, supplies a sufficient margin for reliability. Therefore, the storage electrode height can be reduced by using the high-capacitance HSG-Si electrode with a relatively thick dielectric film, which has sufficient reliability. Such an electrode height reduction simplified the device-fabrication procedure.

The electric reliability of the HSG-Si electrode is shown in Figs.4, 5 and 6. Figure 5 shows a breakdown field distribution for a 6.4 nm-T_{eff} dielectric film, formed on the HSG-Si electrode. The peak of the breakdown-field distribution is sharp and no breakdown failure in low electric fields is observed. A comparison between the result in Figs.4(b) and 4(c) indicates that the leakage current increase, caused by HSG-Si unevenness, is negligibly small. The time-to-breakdown characteristics are plotted in Fig.6 for the HSG-Si and the conventional electrodes. The lifetime of the 6.4 nm-T_{eff} dielectric film on HSG-Si electrodes is sufficiently long, allowing it to survive for 300 years (10^{10}sec) at a 3 V gate voltage.

III.CONCLUSION

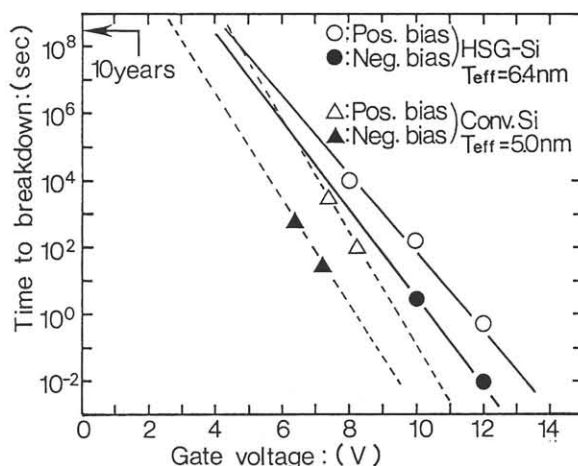We found that the surface of a thin poly-Si film, deposited at 550°C, has hemispherical grains and that its area is twice as large as the area of the films deposited at other temperatures. A specific temperature, 550°C, is the transition temperature of the film structure from amorphous to polycrystalline, producing distinct surface morphology. By applying the HSG-Si film to a storage electrode of a stacked capacitor, twice the storage capacitance can be obtained. The increase in the capacitance makes it possible to reduce the height of the storage electrode, even after using a relatively thick dielectric film for higher reliability. This technique is applicable to the fabrication process for 64Mbit DRAMs.

REFERENCES

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