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Low Temperature Polysilicon TFTs by Non-Mass-Separated Ion Flux Doping Technique

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A low temperature and high throughput self aligned poly-Si TFT fabrication process has been developed. The process includes two key techniques. The first one is a laser induced crystallization of a-Si, occurring in the solid phase, using a high beam scanning speed. The second is a large diameter ion flux doping without mass separation. The maximum processing temperature is 450℃, which is sufficiently low to use inexpensive glass substrates. With this process, excellent poly-Si TFT characteristics of $I_{on}/I_{off}>10^6$ and $\mu_{FE}=40cm^2/Vs$ were obtained.

1. Introduction

High process temperature is one of the most serious problems for the application of poly-Si TFTs to large area liquid crystal displays (LCDs). Several low temperature processes of LPCVD poly-Si of approximately 600℃ have been reported,[1-3] however, this temperature is not sufficiently low for inexpensive glass substrates. Laser crystallization seems to be the most promising method to reduce the process temperature of poly-Si.[4-6]

Parasitic capacitance is another serious problem of large area TFT-LCDs. Self aligned structure is considered to be a good solution to this problem.

We have developed a self aligned poly-Si TFT process with low process temperature and high throughput, using

*Laser induced crystallization of a-Si,

*Large diameter ion flux doping.

2. Laser crystallized poly-Si

Our poly-Si was prepared by laser induced crystallization of PECVD a-Si. Scan speed of the laser beam was an important parameter, and in this study, scan speed of the CW Ar laser beam was 13.0 m/s. This transformation process is a kind of solid phase explosive crystallization that proceeds almost entirely in the solid phase.[7] Crystallization was carried out with unheated substrates in air. Details of experimental conditions were reported previously.[8]

Fig.1(a) is TEM micrograph of a cross section of poly-Si perpendicular to the laser beam scan, showing the grain boundaries to be very obscure. Fig.1(b) shows a plan view in which the grain sizes are small and scattered. The average grain size of about 30nm is estimated from X-ray diffraction analysis (Fig.2). Fig.2 also shows that orientation is very weak. Our poly-Si has a fairly high mobility of $40cm^2/Vs$ despite the small grain sizes and the very weak orientation. The recent work of Serikawa et al.[9] shows that poly-Si with obscure grain boundaries and a columnar structure has very high mobility ($350cm^2/Vs$)

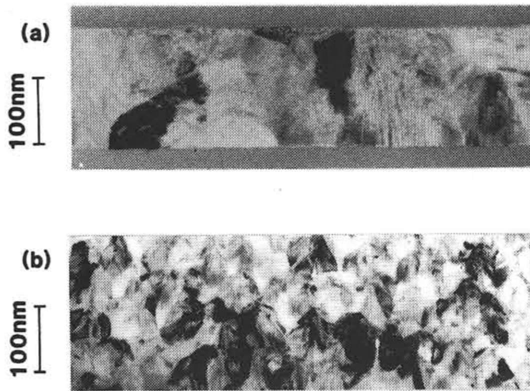

Fig.1 TEM micrograph of laser crystallized poly-Si films. (a) cross section view (b) plan view.

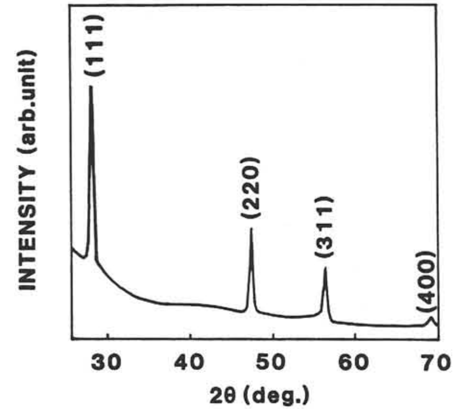

Fig.2 X-ray diffraction patterns of laser crystallized poly-Si film.

in spite of the small grain size. Our poly-Si also has obscure grain boundaries. These high mobilities are thought to be caused by the obscure grain boundaries.

3. Ion flux doping

Source and drain regions of the poly-Si TFTs were formed by non-mass-separated ion flux doping using a bucket type ion source. This ion source had been previously developed as a nuclear fusion ion source and recently has been applied to etching, sputtering, and ion implantation.[10] Yoshida et al.[11] applied a new type ion source using RF discharge and a magnetic field to the formation of source and drain of TFTs. The bucket type ion source is also suitable for ion implantation to TFTs for display use, as it can readily produce high current and large diameter uniform ion flux.[12]

In this study, the source gas was pure PH_3 or 5% PH_3 in hydrogen. The ion flux was extracted from the ion source, accelerated by 2.5-10.0kV, and irradiated directly onto samples without mass separation. Samples were neither heated nor cooled.

Fig.3 shows the depth profile of phosphorus atoms in laser crystallized poly-Si. The source gas is pure PH_3 and the acceleration voltage is 5.0kV. The peak position of phosphorus concentration is shallower than 10nm and this roughly agrees with LSS theory.

Fig.4 shows the sheet resistance of the doped layer versus annealing temperature after doping. At acceleration voltage (Vacc) value of 5.0kV, fairly low sheet resistance of $10^4\Omega/\square$ was obtained with 300℃ annealing. The sample of Vacc=10.0kV requires a higher annealing temperature to reduce resistance. This is presumably due to heavier damages at ion implantation. The samples at Vacc=2.5kV shows somewhat higher resistance than the 5.0kV samples. This is probably because doped layers of 2.5kV samples were thinner than those of the 5.0kV samples.

4. TFT structure and characteristics

Fig.5 illustrates a cross section of a self aligned poly-Si TFT. SiOx, a-Si, and SiON were deposited successively on glass substrates (Asahi AN) by PECVD at 300℃. The SiON was deposited in order to reduce the reflection of the laser beam. After annealing at 450℃ for 30min in N_2 flow for

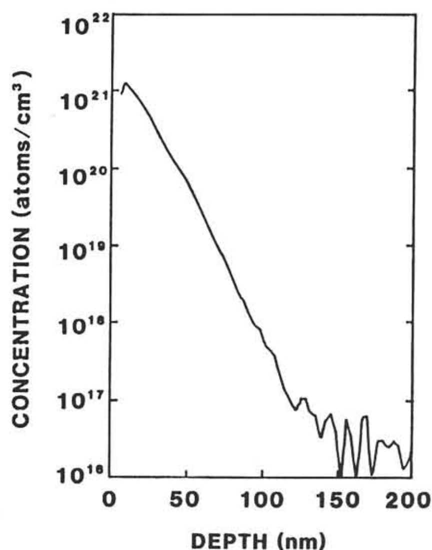

Fig.3 The depth profile of phosphorus atoms in laser crystallized poly-Si.

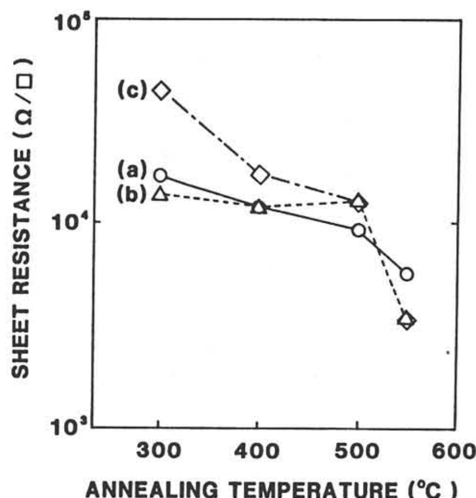

Fig.4 Sheet resistance of doped poly-Si. Activation annealing was carried out for 60min in N_2 flow. (a)Vacc=2.5kV, (b)5.0kV, (c)10.0kV.

the reduction of hydrogen concentration in a-Si, poly-Si lines were formed by laser induced crystallization at room temperature in air. The samples were furnace annealed again (450℃ 60min in N_2 flow), the SiON layer was removed, and the poly-Si was patterned to form islands. Then gate insulator SiNx was deposited by PECVD at 350℃ and Cr gate metal was evaporated and patterned. After dry etching of SiNx, source and drain regions were formed by the above-mentioned ion flux doping. The acceleration voltage was 5.0kV and phosphorus dose was $2x10^{15}$ ions/cm^2. After furnace annealing at 300℃ for 60min in N_2 flow, SiNx was deposited. Contact holes, Cr/Al source and drain metals were formed. Finally SiON was deposited as a passivation layer. The W/L of the channel was 10μm/20μm.

Fig.6 indicates the drain current as a function of gate voltage. Ion/Ioff ratio is greater than 10^6, and the threshold voltage is around 2V. The field effect mobility is around 40 cm^2/Vs, the slope of the subthreshold is about 0.7 V/decade.

Fig.7 shows the drain current versus the drain voltage. A good source and drain contact is achieved.

These self aligned poly-Si TFTs were applied to pixel transistors of LC-TV. The optical performance of the LC-TV shows there are no parasitic capacitance due to gate-drain overlap. The precise results will be reported shortly.

5. Summary

A low temperature and high throughput self aligned poly-Si TFT fabrication process has been developed.

The poly-Si films were formed by laser induced crystallization of a-Si in which small and non-orientated grains were

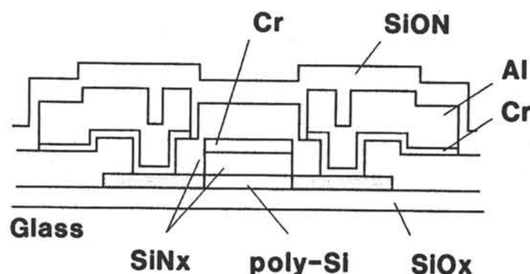

Fig.5 The self aligned poly-Si TFT structure. Poly-Si is 100nm thick and gate insulator SiNx is 200nm thick.

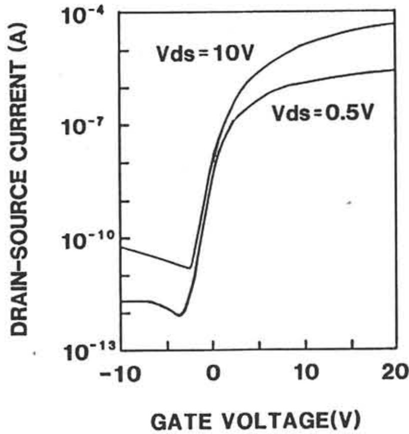

Fig.6 Id-Vg characteristics.

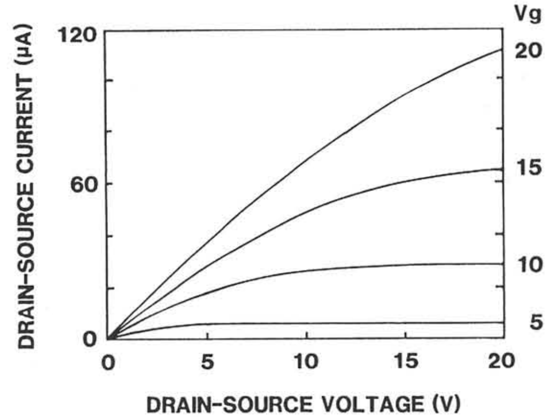

Fig.7 Id-Vd characteristics.

obtained.

The source and drain regions were formed by a new ion flux doping technique which utilize a bucket type ion source with no mass separation. When the acceleration voltage was sufficiently low, low sheet resistance and good ohmic contact were achieved with furnace annealing of 300℃.

The fabricated self aligned poly-Si TFTs show excellent characteristics and were successfully applied to 3.4" diagonal full color LC-TV.

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