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**Invited**

# Modelling and Simulation of TFT-LC Arrays

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The design of TFT/LCD displays requires the trade-off of gate line delay, transistor charging performance, capacitive crosstalk, and other effects which can alter the displayed image. The proper design trade-off will depend on the intended use of the display. A TFT/LCD design system is presented which allows the user to simulate the electrical and optical performance of a TFT/LCD.

## 1. Introduction

Designing the display circuitry of a TFT/LCD requires optimizing both the electrical and optical response of the system. An ideal display would present the desired information without distortion. Real displays must contend with the non-idealities present in any actual design, such as gate line delay or capacitive crosstalk. The trade-offs made in designing a display determine how successfully the display will perform its job. Therefore, the tools used to design and simulate TFT/LC displays should be able to simulate the image that will be produced by the display as well as the details of the electronic response of the system. Standard circuit design software is not capable of simulating the display image, and image processing software is not capable of simulating the electrical behavior of a TFT/LCD. In this work we have combined both circuit design and image simulation into one package to provide a fuller simulation of actual display performance. This design system provides a visible and quantative measure of the benefits and problems of design alternatives, allowing a rigorous approach to optimizing display design.

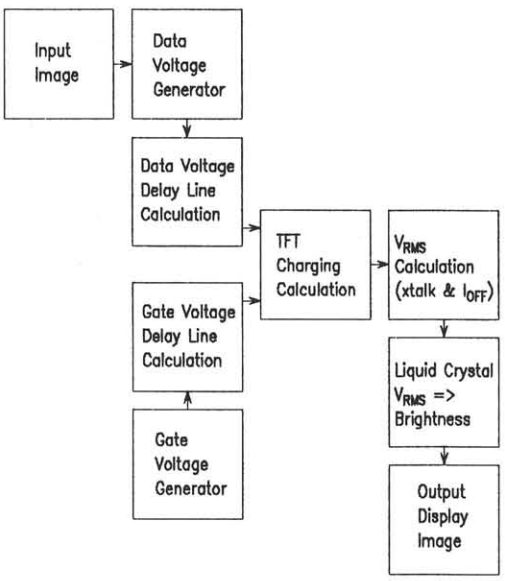


Figure 1. Flowchart of TFT/LCD Electrical and Optical Simulation

Using an input image and the electrical parameters extracted from knowledge of the mask design and the fabrication process, an electrical simulation of the display is performed. The RMS value of the unit cell voltage is used to determine the brightness of each unit cell.

## 2. TFT/LCD Design and Simulation System

The TFT/LCD simulation system calculates the relevant electrical and optical parameters of display performance. The outline of the simulation process is shown in figure 1. The

simulator takes the data in the input image through each of the steps that occurs in the actual display. The computation is performed on one unit cell at a time, building up to the final image.

First the input image data is converted into the proper data voltages. For this step a look up table is used, which is analogous to the gamma correction processing that would occur in an actual display.

The gate and data voltage generators model the drive circuits that are external to the active array area. From these sections come the time dependent voltage waveforms that would be seen coming from the drive circuitry.

A top view of a unit cell in a display is shown in figure 2. The gate line that controls the access transistor is located at the bottom of the drawing; another gate line or reference line is shown at the top of the drawing providing the counter electrode for the storage capacitor. The data line for this cell runs down the left hand side of the figure. The data line crosses over the gate line in every cell of the display. The delay line calculator[1] models the pulse delay characteristics of the gate and data lines in the display. If the values of the delay line elements are fixed in the model, the telegraph line equation can be used. The resistance of the delay lines is the resistance of the metal lines themselves. The capacitance of the lines includes the capacitance of the crossovers, the capacitance of the drain of the transistor, the capacitance to the front plate, and the series combination of the storage capacitor and the liquid crystal capacitance. The output of this section shows the voltage amplitude reduction and time delay that are caused by the delay lines. For many displays the data line delay is quite small ( < 100 nS ); the effect of the data line delay can then be neglected without seriously affecting the accuracy of the simulation.

The TFT charging section models the transistor charging[2] of the unit cell capacitance. The equivalent circuit used to model the charging of the unit cell is shown in figure 3.

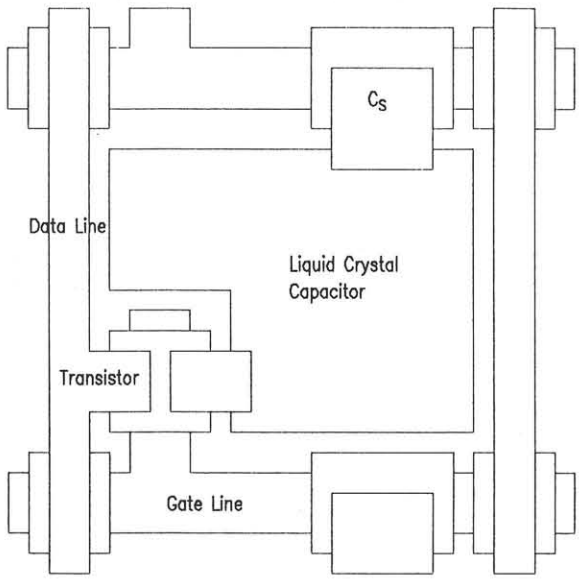


Figure 2. Top View of Typical Unit Cell
The mask layout of a unit cell of the display is shown. The gate line is used to turn the transistor on and off. The data line provides the voltage value for the accessed cell. The adjacent line is used as a reference voltage for the storage capacitor.

The previously developed gate and data voltage waveforms are used along with the present value of the unit cell voltage to perform the calculation. Charge pumping caused by the gate line voltage drop is modelled by taking 1/2 of the channel capacitance and the gate source capacitance as a lumped element which is tied between the gate and the pixel connection of the transistor[3]. The value of the liquid crystal capacitance depends upon the previous frame's RMS bias level. Because the rate of liquid crystal response is much slower than the charging time of the cell (milliseconds of liquid crystal response time versus microseconds of charging time), the liquid crystal capacitance is held fixed throughout the charging time.

With the unit cell capacitors charged and the transistor biased off, the equivalent circuit shown in figure 4 is used to model the root-mean-square (RMS) voltage on the liquid crystal capacitor during the rest of the

frame time. The optical behavior of twisted nematic liquid crystals is well modelled by looking at the transmitted light as a function of the RMS voltage across the cell.

The liquid crystal in the cell and the layers used on either side of the cell for passivation and alignment are modelled as three parallel RC circuits in series. The capacitance and resistance of the liquid crystal cell determine the decay time of the voltage across the liquid crystal. Liquid crystal processing technology has developed to the point where this decay time is much longer than the frame time (15 mS to 20 mS) of typical displays.

The capacitors $C_{PD}$ and $C_{PDA}$ provide a crosstalk path between the voltage variations of the data line and the voltage across the liquid crystal cell[4]. The capacitive voltage divider causes the instantaneous voltage across the liquid crystal to change according to the other data voltages that are present on the two data lines adjacent to the liquid crystal capacitor flag, causing a change in the RMS voltage across the liquid crystal. Typically, the voltage across the liquid crystal capacitor can be changed by a few percent by capacitive crosstalk. In general, alternating data line voltages reduces the visibility of this effect.

The resistor $R_{TFT}$ in figure 4 represents the OFF state resistance of the transistor. Typically the value of this resistance is several Tera-Ohms when the transistor is in the dark, but exposure to light can reduce this resistance to several Giga-Ohms. When the off resistance of the cell is low, the charge lost through transistor leakage must be calculated.

The RMS voltage across the liquid crystal is converted to brightness by using a lookup table describing the liquid crystal to be used in the display. The values in the lookup table can be experimentally determined or they can be the result of additional numerical simulation. For large area displays the effect of viewing angle upon the shape of the voltage to brightness conversion must be considered. A lookup table for each viewing angle must be constructed, and the proper viewing angle for each unit cell must be calculated to properly simulate the actual appearance of the display.

The resultant image can be viewed on a high resolution CRT or printed using a grayscale color printing medium. This image represents a simulation of how the actual display would appear.

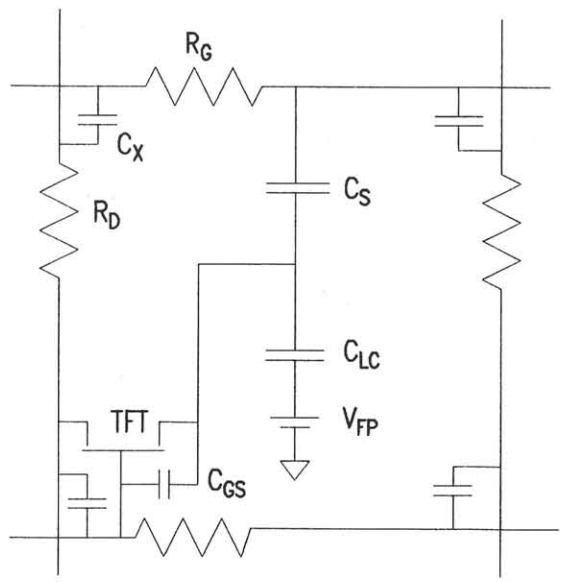


Figure 3. Unit Cell Charging Equivalent Circuit

The equivalent circuit used to model the charging operation is shown. The gate voltage delay line and data voltage delay line are shown. The transistor used to charge the pixel includes the gate to source capacitance of the transistor. The capacitance of the liquid crystal capacitor depends upon its RMS bias voltage.

## 3. An Example - Transconductance, Gate Threshold Interaction

An example of the use of this simulation system is shown in figure 5. A case has been chosen where the design of the unit cell is fixed and where the designers would like to understand the tolerance of the design to variations in transistor threshold voltage and channel mobility. A small segment of a display is simulated which shows 8 gray levels, producing an image for a region of the display. An array of these simulations has been composed showing the effect of changes in threshold voltage and mobility.

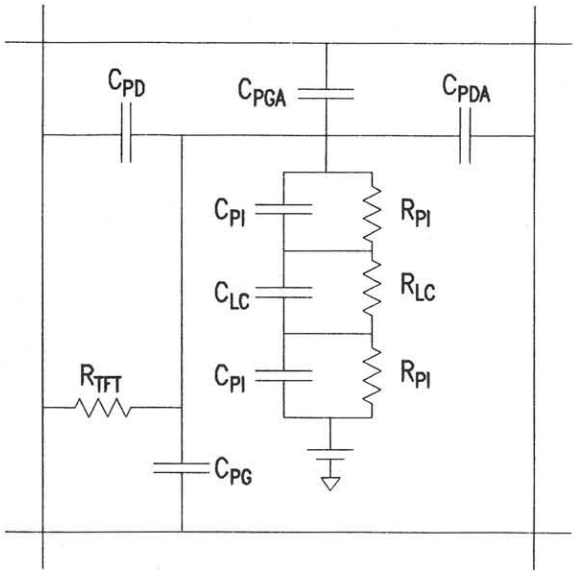


Figure 4. Unit Cell Holding Equivalent Circuit

The equivalent circuit used to model the holding operation is shown. The liquid crystal cell is modelled by three RC circuits in series. The capacitors Cpd and Cpda are used in the calculation of capacitive cross-talk from the data lines. The resistor Rtft is used to model the off resistance of the transistor.

Figure 5. Gate Threshold Voltage and Mobility Dependence of Display

The simulation technique has been used to determine the display image quality as a function of the gate threshold voltage and the mobility of the TFT. The unit cell design is fixed in this simulation. Horizontally the image consists of eight equally spaced gray levels. The image is repeated ten time across the figure, with the gate threshold voltage changing by one volt between each repetition. Vertically the image is also repeated 10 times, with the mobility used to calculate each of the images changing from 0.2 to 1.1 cm. squared per volt - sec.

1) R. Wisnieff; Proc. of the SID, Vol. 29/2 (1988) 173.

2) W. E. Howard; Proc. of the SID, Vol. 27/4 (1986) 313.

3) D. E. Castleberry, George E. Possin; SID 88 Digest (1988) 232.

4) W. E. Howard et al; IDRC 1988 Digest (1988) 236.