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Optical Characteristics Simulation of TFT Addressed Liquid Crystal Display

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A simulation method is described to calculate characteristics such as optical threshold voltages and contrast ratio in TFT-LCDs. The model accuracy was verified by comparing with measurements for a 10-inch diagonal LCD addressed by a-Si TFTs. Contrast ratio distribution in an LCD was also investigated. One of the nonuniformities was attributed to the decrease in voltage drop, due to the gate-source parasitic capacitance with increasing gate voltage fall time.

1. INTRODUCTION

As the size of thin film transistor addressed liquid crystal displays (TFT-LCDs) is increased, uniformity of the display quality should be considered. Distribution of optical characteristics along the gate line direction (X-direction) has been reported [1], where nonuniformity was attributed to the decrease in the charged voltage through TFTs with increasing gate voltage rise time along the direction. As for the distribution along the scanning direction (Y-direction), it has been discussed as a function of off-state current in TFTs [2]. The voltage drop effect by the gate-source parasitic capacitance (C_{GS}), however, has not been examined.

In this paper, the simulation method was developed, and the effect on contrast ratio distribution (both X- and Y-directions) by the increase of gate line resistance or off-state current was calculated.

2. SIMULATION METHOD

Figure 1 shows an equivalent circuit describing a picture element. Here, C_{STG} is the storage capacitance, installed in parallel to the LC capacitance (C_{LC}), and R_{LC} is the LC resistance. C_{GS} is the parasitic capacitance between gate and source electrodes in a TFT.

Figure 2 plotts a voltage wave form diagram using frame reversed driving method. The subscripts H and L denote high and low levels of each terminal voltage, respectively. The root-mean-square-voltage (Vrms) applied to the LC was determined by calculating V_S, which was described as the following three characteristics. First, the drain voltage is charged to C_{LC}, while the gate voltage (V_{GH}) with the period of t_L is applied. The voltage of (V_{DH} - V_{DL})/2 is designated as the signal voltage (Vsig). Next, the charged voltage (V_S) shift with the voltage drop ΔV at the time of the gate voltage fall due to C_{GS} coupling, and then the TFT is turned off. Finally, V_S is stored until another gate voltage is applied for the reversed voltage (V_{DL}).

2.1 Charging Characteristics

The equation describing the charging characteristics is given as

$$(C_{LC}+C_{STG})\frac{d}{dt}(V_S(t)-V_{COM}) = I_{on} \quad . \quad (1)$$

Here, Ion is on-state current in the TFTs, which was obtained by a gradual channel approximation [3].

2.2 Storage Characteristics

The storage characteristics for charged voltage are described as

$$\frac{V_S(t)-V_{COM}}{R_{LC}}+(C_{LC}+C_{STG})\frac{d}{dt}(V_S(t)-V_{COM})=I_{off} \quad . (2)$$

Here, Ioff, which depends on the terminal voltages, is off-state current and was obtained by measurements with a test element.

2.3 Voltage Drop

The voltage drop caused by the non-distorted gate pulse is expressed as

$$\Delta V_{GS} = \frac{C_{GS}}{C_{GS}+C_{LC}+C_{STG}}(V_{GH} - V_{GL}) \quad . \quad (3)$$

The C_{LC} depends on Vrms because of the anisotropy of LC-permittivity, while C_{GS} depends on the voltage (V_{GH}-V_D) because channel resistance in its MIS structure varies with the voltage. The C_{GS} dependence was estimated from the measured voltage drop for TFT test elements.

For actual LCDs, V_{GS} is smaller than that expressed by eq. (4) because re-charging to the V_D level happens during the gate voltage distortion time. The gate pulse distortion in the distributed element circuits having R and C elements was obtained analytically [1], and the re-charging effect was considered.

Temperature dependences for mobility and threshold voltage in TFT characteristics or LC-resistance were fitted to measurements.

3. RESULTS AND DISCUSSION

3.1 Accuracy of Simulation

To verify the simulation accuracy, the calculations were compared with measurements for a 10-inch diagonal LCD addressed by a-Si TFTs.

Figure 3 shows gate pulse width (t_L) dependence of the optical threshold voltages (Vth_{50}, Vth_{10}) at low temperature. These voltages denote the value of Vsig showing 50% or 10% transmittance. Both rose markedly by shortening the pulse width to less than 20 μs, because the charging rate was decreased.

Figure 4 shows frame frequency (f_F) dependence of these threshold voltaged at high temperature. The voltages rose gradually with decreasing f_F (increasing storage time), because the stored voltage decreased.

Good agreement between calculation and measurement was obtained in practical temperature range (0-60℃). This agreement verified the simulation accuracy for designing TFT-LCDs.

3.2 Uniformity of Display Area

Figure 5 shows the contrast ratio (CR) distribution in an LCD calculated under different values of gate line resistance (R_G) and TFT off-state current (Ioff). The uniformity obtained for low R_G of 1kΩ and low Ioff of $5X10^{-13}$A was fair (Fig. 5 (a)), whereas the ratio decreased with increasing Y-distance for high Ioff of $5X10^{-11}$A (Fig. 5 (b)). This decrease was attributed to variation in the driving conditions: the V_D at the first gate line (Y=0mm) was constant during the storage time and the difference between V_S and V_D was small, while the V_D at the final line (Y = 160mm) was immediately reversed after the gate voltage fell, which gave a larger voltage difference between both voltages. The larger voltage difference caused the stored V_S to decay and Vrms decreased with increasing Ioff.

The ratio calculated for high R_G of 10kΩ decreased with increasing X-distance from the left side on which the gate pulse was supplied, and CR had a sharp peak along the left edge (Fig. 5 (c)). This anomalous distribution

possibly resulted from the decrease of Vrms due to the increase of V_G distortion.

To investigate the relationship between Vrms and the gate pulse distortion, position dependence of charged source voltage (V1) for V_{DH} was compared with that of ΔV_H or ΔV_L shown in Fig. 6. The gate voltage fall time (t_{GF}) is also plotted. The t_{GF} increased with increasing distance and then tended to saturate at about the center of the LCD. ΔV_L decreased similar to t_{GF}, while the other value was almost constant. If charging and storage characteristics are perfefct, Vrms is expressed simply as

$$Vrms = Vsig + \Delta V_L - \Delta V_H \qquad (4)$$

This equation indicates that Vrms decreases with decreasing ΔV_L when ΔV_H is constant. Thus the decrease in the CR farther along the gate line from the driven end was attributed to the ΔV_H decrease.

To verify the X-distance dependences of ΔV_H and ΔV, the voltage drop ΔV was measured for a TFT test element as shown in Fig. 7, where the parameter t_F simulated the gate fall time in some actual LCDs. Each gate-drain voltage (V_{GD}) of 5 V or 20 V corresponded to the actual driving conditios in the positive or negative phases (ΔV_H or ΔV_L). The voltage drop ΔV for V_{GD}=20V decreased with increasing t_F, while ΔV was constant with V_{GD} of 5V. These t_F dependences in this measurement showed a similar tendency to the calculation in Fig. 7.

It was found that the voltage drop was decreased by the increase of the gate voltage fall time, and had a significant influence on the distribution of optical characteristics.

4. CONCLUSION

A comprehensive model which simulates the distribution of optical characteristics in TFT-LCDs was developed by considering the distortion of gate voltage. The accuracy of the model was verified by comparing with measurements in a practical temperature range (0-60℃). Uniformity analysis indicated that the high resistance of the gate line resulted in a contrast ratio peak at the driven end of the gate line. This anomalous distribution was attributed to the decrease in voltage drop in the negative phase due to the gate pulse distortion.

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1) R. L. Wisnief; Proc. SID 29(1988) 173.
2) K. Ono et al.; submitted to Trans. IEICE.
3) Y. Kaneko et al.; IEEE Trans. Electron Devices 36(1989) 2953.

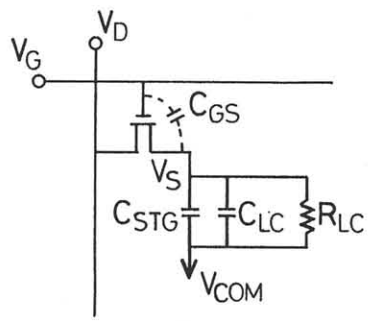

Fig.1 Equivalent circuit for a picture element.

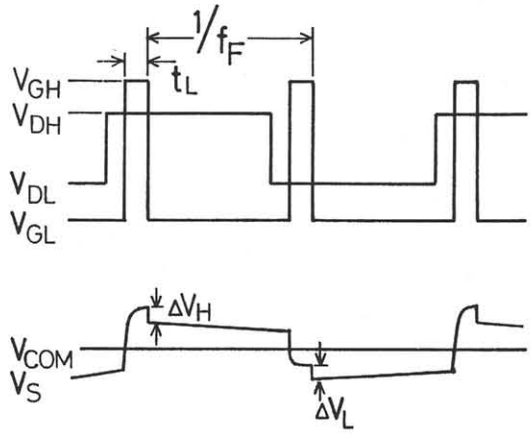

Fig.2 Drive voltage timing chart.

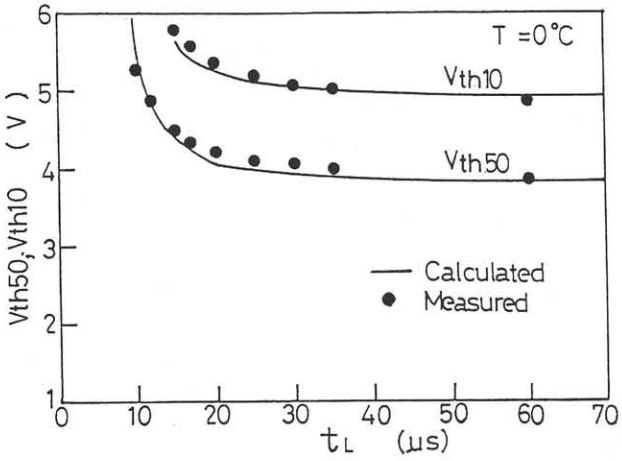

Fig.3 Optical threshold voltage versus gate pulse width.

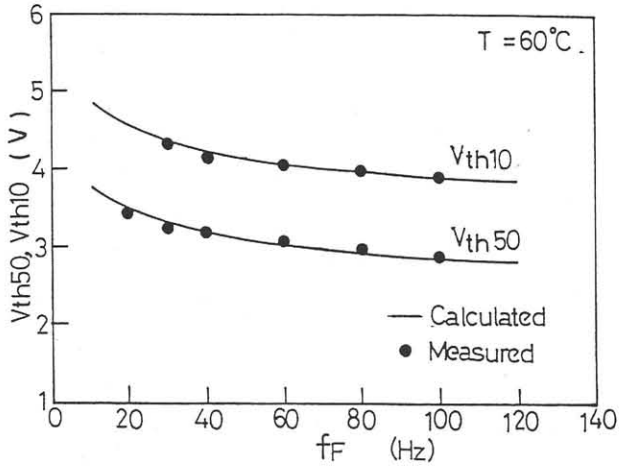

Fig.4 Optical threshold voltage versus frame frequency.

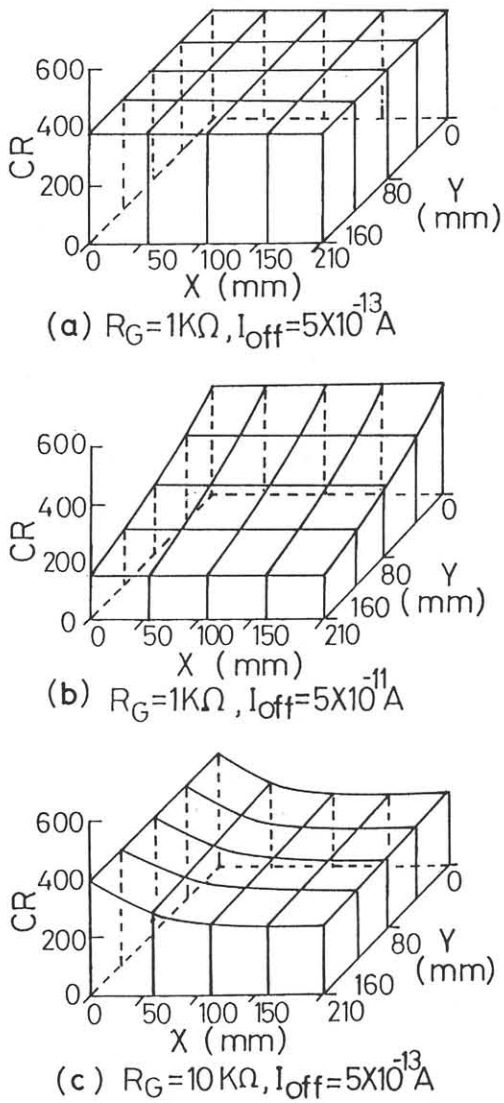

Fig.5 Contrast ratio distribution calculated under different values of gate line resistances and TFT off-state currents.

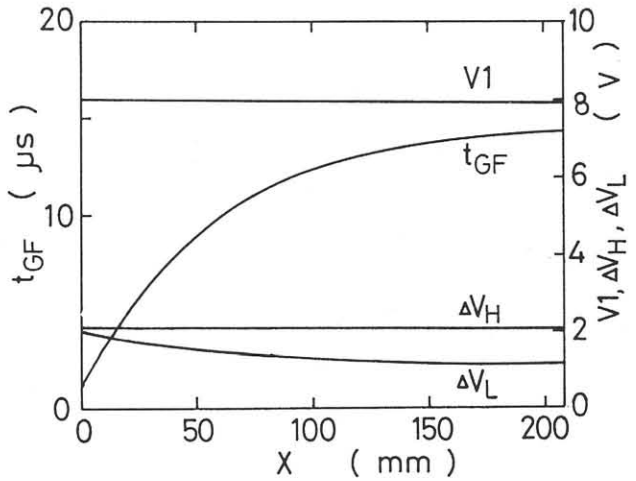

Fig.6 Calculated distributions of gate voltage fall time, charged voltage, and voltage drops along a gate line.

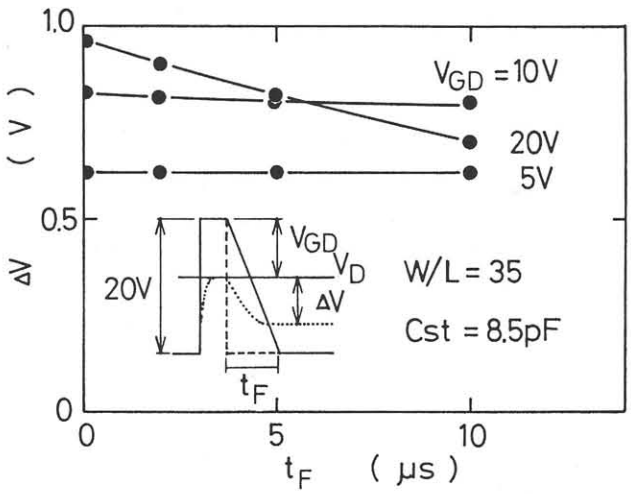

Fig.7 Measured voltage drops vs simulated gate voltage fall time.