

## The Optimum Design of TFTs by the Dynamic Characteristics Measurement

Tsutomu YAMADA, Susumu OHIMA, Katsuya KIHARA, Yushi JINNO  
 Yuji OKITA, Teiji ARIOKA, Takao YAMAGUCHI, and Takashi NAKAKADO  
 Semiconductor Research Center  
 SANYO Electric Co., Ltd  
 809 Takamaru, Higashi-Tarumi  
 Tarumi-ku, Kobe 655 Japan

By measuring the voltage from the source electrode of the TEG-TFTs, the dynamic characteristics of TFT-LCDs have been analysed. It was clearly determined that the  $V_{rms}$  decrement depends on the increase in the delay time of the gate signal. Under the H-Reversed Halfline driving method, the time lag between the drain and the gate signal, and the size of TFTs were both optimized. We were able to obtain these results on the condition that  $\tau_{delay}$  was as 1/3 the on-time of the gate signal.

### 1. Introduction

Recently, Liquid Crystal Displays addressed by amorphous silicon thin film transistors (TFT-LCDs) have received a great deal of attention and have been widely applied to OA terminal displays<sup>1)</sup> and video projectors<sup>2) 3)</sup>, etc., because they enable large-area, high-quality and high-resolution color displays. In the near future, as the demands for these performances will increase the optimum design of TFTs becomes more important. Up to now, the dynamic characteristics have been estimated indirectly by means of transmittance versus applied voltage (V-T) characteristics<sup>4)</sup>.

The H-Reversed driving method, in which the polarity of video signals is reversed in each scanning line, is generally used to obtain flicker-free displays. In this case, however, the picture quality of TFT-LCDs deteriorates because of many factors, such as the delay time of the gate signal ( $\tau_{delay}$ ) and the time lag between the drain and the gate signal (Tgd), etc. In this paper, we have clearly explained the

mechanisms for this, and have also optimized the driving conditions and the size of TFTs by directly measuring the dynamic characteristics<sup>5) 6)</sup>.

### 2. Measuring method

We used TEG (Test Element Group)-TFTs, which are about 100 times as large as the original TFTs (W/L). A storage capacitor for pixel capacitance is connected to the source electrode, and the source voltage is measured directly by using a voltage follower circuit. Fig. 1 shows the block diagram of the TFT Dynamic Characteristics Measurement System. The driving waveform used in this experiment is shown in Fig. 2. Based on the NTSC Halfline driving method, the gate signal ( $V_g$ ) is a pulse with a field period ( $T_f$ ) of 1/60 sec and an on-time ( $T_{on}$ ) of about 60  $\mu$ sec.  $V_c$  is a DC voltage applied to the opposite side of the storage capacitor. Tgd is the time lag between the drain and the gate signal.  $\tau_{delay}$  is the time required for the gate signal to decline from 100% of maximum amplitude to 10%. The

dependence of the TFT-LCDs dynamic characteristics on  $\tau_{\text{delay}}$  and  $T_{\text{gd}}$  are measured for many dummy capacitances.

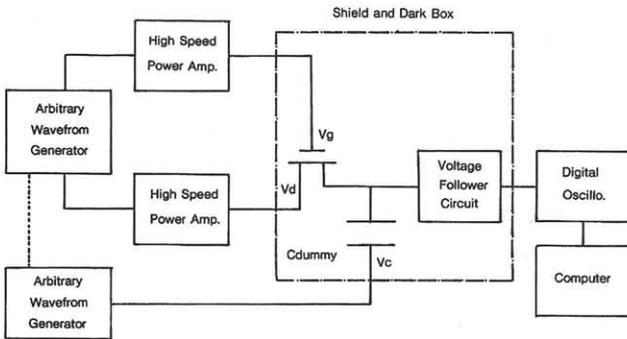


Fig. 1 The block diagram of the TFT Dynamic Characteristics Measurement System.

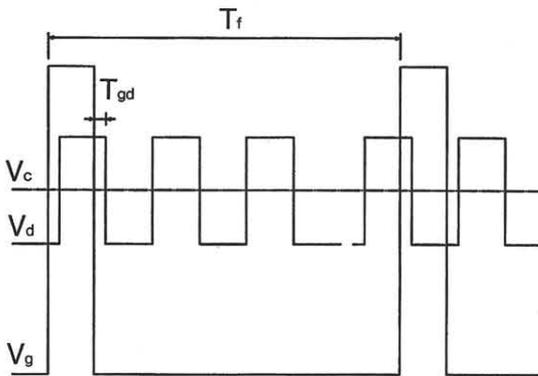


Fig. 2 The driving waveform based on the H-Reversed NTSC Halfline driving method.

### 3. Results and Discussion

In this experiment, we defined  $\tau_{\text{on}}$  as a parameter for charging. This is expressed by

$$\tau_{\text{on}} = R_{\text{on}} C$$

where  $R_{\text{on}}$  is the on-state resistance of TFT at  $V_g = 7.5\text{V}$ ,  $V_d = 3\text{V}$ , and  $C$  is the dummy capacitance. Fig. 3 shows  $\tau_{\text{delay}}$  dependence of the relative ratio of the effective voltage to the applied voltage ( $V_{\text{rms}}/V_{\text{in}}$ ), the charging ratio and the holding ratio.  $\tau_{\text{on}}$  is about  $16 \mu\text{sec}$ . On the condition that

$T_{\text{gd}}$  is constant, the  $V_{\text{rms}}$  decreases when  $\tau_{\text{delay}}$  is larger.

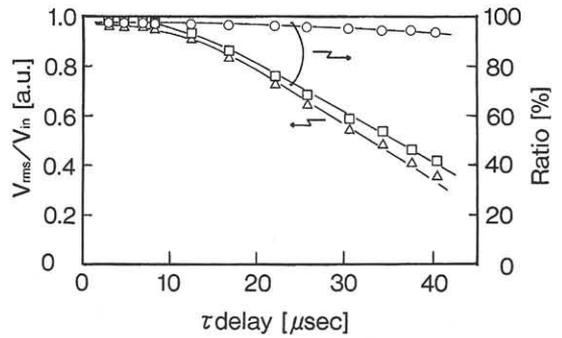


Fig. 3  $\tau_{\text{delay}}$  dependence of the  $V_{\text{rms}}/V_{\text{in}}$ , the charging ratio and the holding ratio.  $\triangle$ ,  $\circ$  and  $\square$  are measured points for the  $V_{\text{rms}}/V_{\text{in}}$ , the charging ratio and the holding ratio.  $\tau_{\text{on}}$  is about  $16 \mu\text{sec}$ .  $T_{\text{gd}}$  is  $2.6 \mu\text{sec}$ .

As shown in Fig. 3, the charging ratio slightly decreases but the holding ratio decreases dramatically. We realized that the main cause of the  $V_{\text{rms}}$  decrease is not a reduction in the charging ratio but rather inferior off-state characteristics. Detailed observation of the discharged waveforms made the mechanisms for these inferior off-state characteristics clear.

Fig. 4 shows the waveforms of the source voltage in the positive period ( $V_d(+)$ ) and the negative period ( $V_d(-)$ ), when  $\tau_{\text{delay}}$  is about  $20 \mu\text{sec}$  (solid line). It also shows the source voltage when  $\tau_{\text{delay}}$  is  $0 \mu\text{sec}$ , for comparison (broken line).  $\Delta V$  is the difference of the source voltage. When  $\tau_{\text{delay}}$  is  $20 \mu\text{sec}$  the charging ratio is a sufficient value ( $>95\%$ ) within  $T_{\text{on}}$ . At the falling gate signal, leakage current is large because the TFTs have not completely reached an off-state, and the drain voltage changes, so the source voltage is discharged to the drain electrode. When  $\tau_{\text{delay}}$  is  $0 \mu\text{sec}$  these inferior off-state characteristics are not observed. These characteristics are more noticeable in the

negative period, that is,  $\Delta V$  is larger than in the positive period. Fig. 5 shows  $T_{gd}$  dependence of the  $V_{rms}/V_{in}$  on the constant  $\tau_{delay}$ . Under these conditions, the  $V_{rms}$  takes a maximum value in the optimum  $T_{gd}$ . As  $T_{gd}$  is smaller than the optimum value, the  $V_{rms}$  decreases because of inferior off-state characteristics. And as  $T_{gd}$  is larger than the optimum value, the  $V_{rms}$  decreases because of the charging ratio reduction. That is to say, we are able to maximize  $V_{rms}$  by optimizing  $T_{gd}$ .

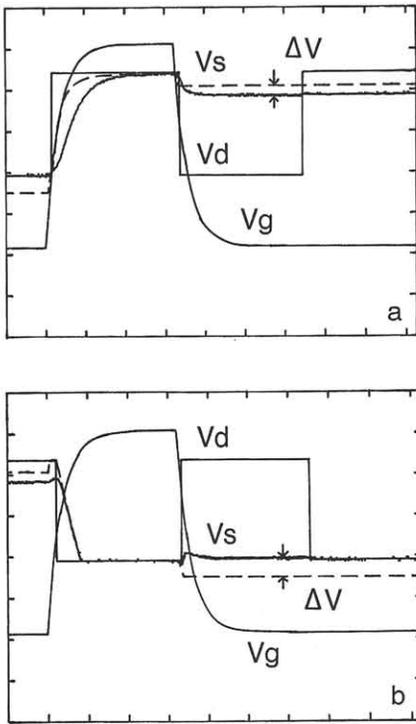


Fig. 4 The waveforms of the source voltage for  $\tau_{delay}$  ; 20  $\mu\text{sec}$  (solid line) , 0  $\mu\text{sec}$  (broken line) in the positive period ( $V_d(+)$ ) (a) and the negative period ( $V_d(-)$ ) (b).  $\Delta V$  is the difference of the source voltage.

Fig. 6 shows  $\tau_{on}$  dependence of  $V_{rms}/V_{in}$  at the optimum  $T_{gd}$ . The maximum value of the  $V_{rms}$  decreases as  $\tau_{on}$  increases. Although off-state characteristics can be improved by optimizing  $T_{gd}$ , the charging ratio decreases because the effective charging time becomes shorter. We are thus able to determine the

maximum  $\tau_{on}$  to obtain a  $V_{rms}$  value which is nearly equal to the applied voltage.

Consequently, we are able to determine the optimum  $T_{gd}$  and the size of TFTs on the condition that  $\tau_{delay}$  is as large as 20  $\mu\text{sec}$ .

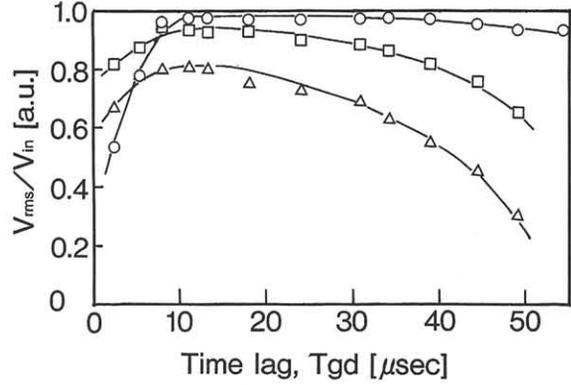


Fig. 5  $T_{gd}$  dependence of the  $V_{rms}/V_{in}$ .  $\circ$  ,  $\triangle$  and  $\square$  are measured points for  $\tau_{on}$  ; 5, 25, 50  $\mu\text{sec}$ .  $\tau_{delay}$  is about 20  $\mu\text{sec}$ .

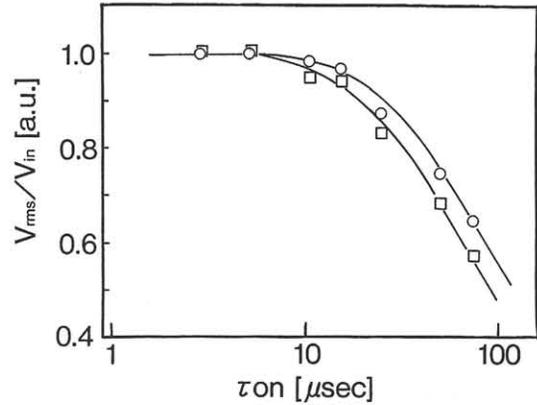


Fig. 6  $\tau_{on}$  dependence of the  $V_{rms}$ .  $\circ$  and  $\triangle$  are measured points for  $\tau_{delay}$  ; 0, 20  $\mu\text{sec}$ .  $T_{gd}$  is the optimum value for each  $\tau_{on}$ .

#### 4. Conclusion

Using the method for measuring dynamic characteristics, we showed the dependence of the effective voltage ( $V_{rms}$ ) on the delay time of the gate signal ( $\tau_{delay}$ ), the time lag between the drain and the gate signal ( $T_{gd}$ ), and the size of TFTs ( $W/L$  and/or pixel capacitance). The mechanisms for this

dependence were made clear and the optimum design of TFT-LCDs was devised.

When  $\tau_{\text{delay}}$  is large, the  $V_{\text{rms}}$  applied to the storage capacitor decreases, which is the main cause of inferior off-state characteristics. These characteristics are caused by increments of leakage current which occur at the falling gate signal because the drain voltage changes before the TFTs have completely reached the off-state. Optimizing  $T_{\text{gd}}$ , the  $V_{\text{rms}}$  reaches a maximum value, and this maximum value depends on the size of TFTs.

In the near future, TFT-LCDs will tend to be larger in size and of a higher resolution, so the resistance of the gate bus line will naturally increase. Using our method, we are able to determine and design the optimum  $T_{\text{gd}}$  and the optimum size of TFTs.

## 5. References

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