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Numerical Simulations of Amorphous and Polycrystalline Silicon Thin-Film Transistors

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In this paper we present results of two-dimensional numerical simulations of both amorphous silicon and NMOS and PMOS polycrystalline silicon thin-film transistors. Both types of devices are modeled using an effective medium approach whereby the defects and grain boundaries in the material are treated as a spatially uniform density of localized states in the band gap. The field-effect mobility is self-consistently calculated from the appropriate band mobility and using one set of parameters for each material we obtain good agreement between simulations of both output and transfer characteristics and experimental data.

1. INTRODUCTION

We have developed a two-dimensional numerical simulation tool to predict the behaviour and analyze the device physics of both amorphous silicon (a-Si) and polycrystalline silicon (p-Si) thin film transistors (TFTs). Our effective medium model assumes a spatially uniform density of localized states in the band-gap of both materials. The dependence of the field-effect mobility on gate voltage is therefore controlled by the distributions of tail states near the band edges. The model requires a user specified device geometry and the appropriate material properties of each layer. The computer then solves both Poisson's equation and the carrier continuity equations. For a-Si TFTs, using one self-consistent set of parameters we have modeled conventional low voltage, high voltage and vertical structures [1].

By changing the density of states (DOS) and carrier band mobilities we have adapted our a-Si model to describe both NMOS and PMOS polysilicon TFTs. The significant difference between the physics of the two technologies is that the output characteristics of the p-Si devices exhibit a "kink effect" at high drain voltages due to impact ionization or other high field carrier generation mechanisms which do not occur in a-Si devices. The field-effect mobility of the p-Si devices is approximately two orders of magnitude higher than in an a-Si TFT.

2. AMORPHOUS SILICON TFTs

In Figure 1 we show the density of localized states for undoped a-Si. Also shown is a second distribution where the density of both deep and exponential tail states in the upper half of the gap has been doubled. In Figure 2 we show computed transfer data for an electron band mobility of 13 cm^2/Vs for the normal DOS and doubled DOS together with experimental data. We see excellent agreement between the model and experimental data showing the validity of our DOS spectrum. The presence of tail states near the conduction band edge leads to the field-effect mobility being around 1 cm^2/Vs at normal operating voltages but it is also weakly dependent on the gate voltage [2], increasing as the Fermi level is moved closer to the conduction band (higher gate bias). Doubling the density of deep states reduces the
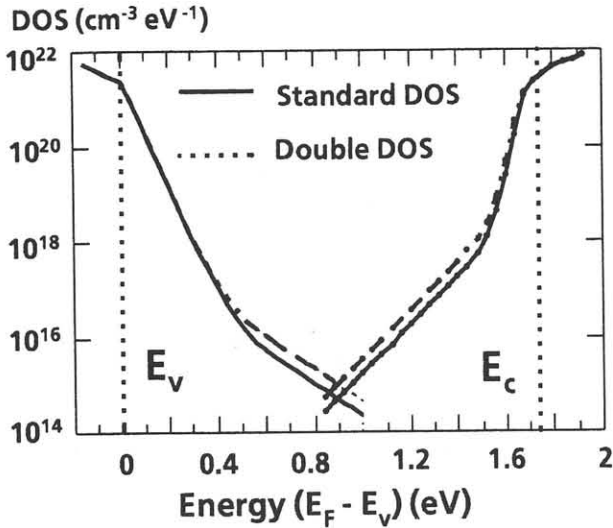
DOS (cm^{-3} eV^{-1})

Fig. 1 Density of states (DOS) for undoped amorphous silicon. Also shown is a distribution with double the density of deep states
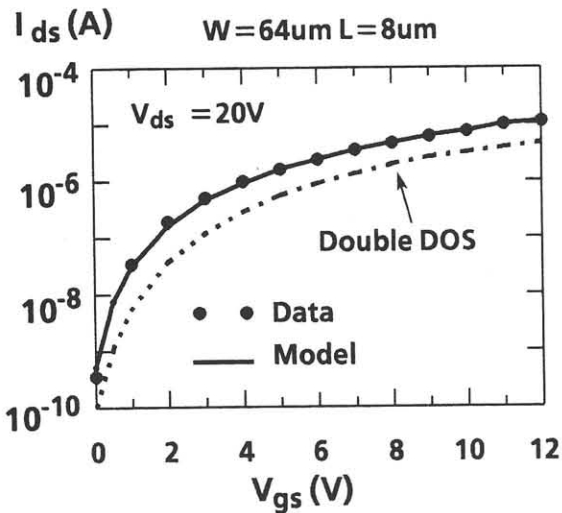

Fig. 2 Computed and experimental transfer data for a-Si TFT for standard and increased DOS

increases the threshold voltage by about 2V. This shows the sensitivity of our results to the DOS and also shows that the distribution shown in Figure 1 is within a factor of two of experimental data.

In Figure 3 we see computed and experimental output characteristics for an a-Si TFT. The good agreement relies on a new model for the metal - n+ contacts where the contact
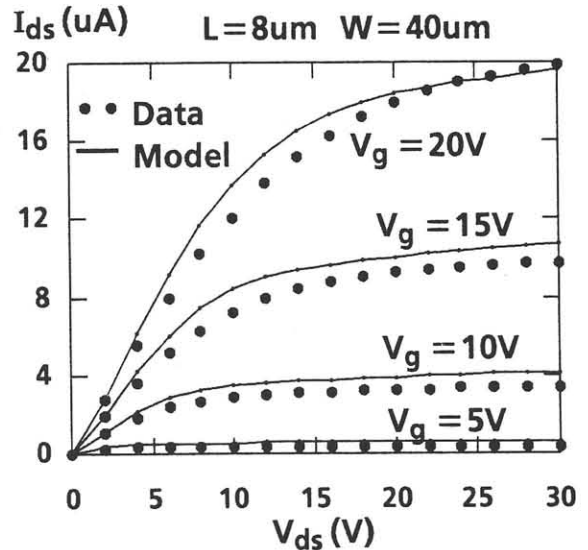

Fig. 3 Computed and experimental output data for a-Si TFT

resistance decreases with increasing current flow. In Figure 4 we show computed and
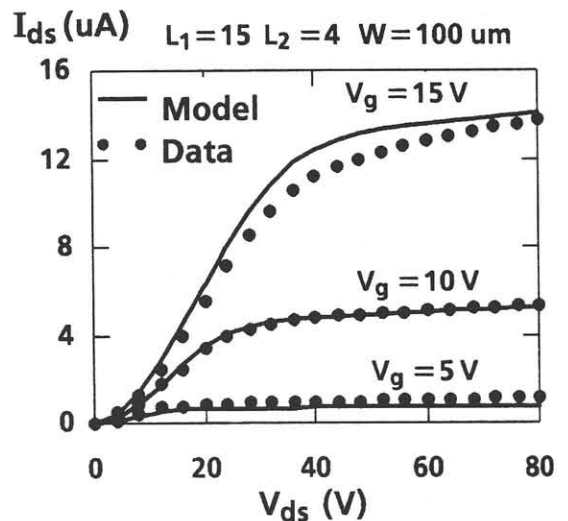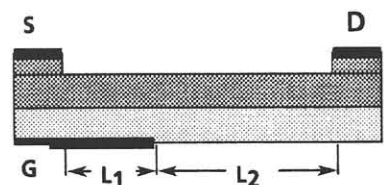

Fig. 4 Computed and experimental output data for a-Si high voltage TFT shown below.

experimental output characteristics for an offset drain high voltage a-Si TFT [3]. At low V_{ds}

1000

current flow is determined by space-charge limited current flow in the ungated region of length L_2 , leading to the apparent current crowding near the origin. At higher values of V_{ds} the current flow is limited by the accumulation channel formed above the gated region at the silicon dielectric interface, causing the device to saturate. The good fit to the data is very dependent on the DOS in the a-Si, further validating our model.

3.   POLY- SILICON TFTs

To simulate polysilicon TFTs we have assumed that we can model the material as spatially uniform, and therefore the effects of grain boundaries are included as an average density of traps. This approach enables the field-effect mobility to be self-consistently calculated from the band mobility, and predicts its correct dependence on gate field. The derived state distribution for polycrystalline silicon is shown in Figure 5. This has been
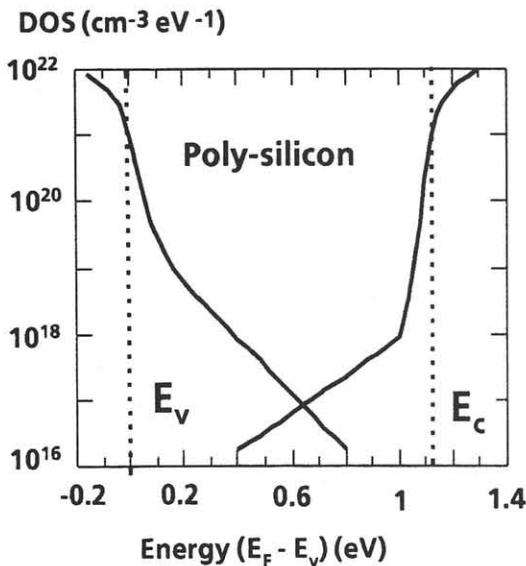
DOS (cm⁻³ eV ⁻¹)

Fig. 5   Effective density of states for polysilicon

determined by fitting the subthreshold characteristics of both PMOS and NMOS devices

to the experimental data shown in Figure 6. Further confirmation of this approach is provided from measurements of the activation energy of the source-drain current as a function of gate bias for these TFTs. Our model fits this data extremely well, showing that this activation energy can be interpreted as the energy difference between the Fermi level and the band-edge in the p-Si channel, as opposed to an effective grain barrier height [4]. These
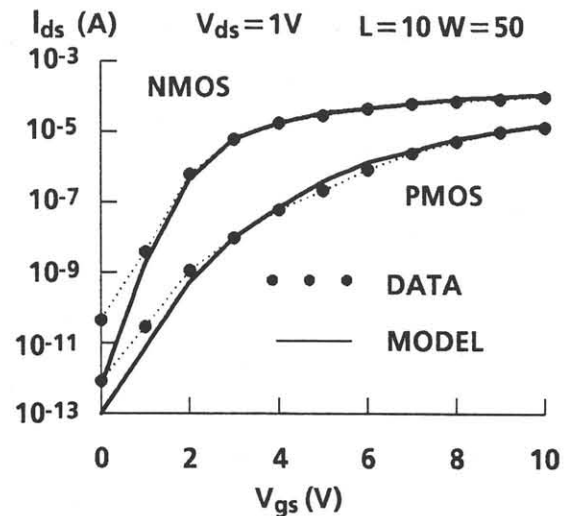
Fig. 6   Computed and experimental subthreshold characteristics for NMOS and PMOS p-Si TFTs. All voltages are negative for PMOS devices.

results have also enabled us to determine the effective carrier band mobilities in p-Si , 150 cm²/Vs for electrons and 120 cm²/Vs for holes.

Another important difference in the physics of a-Si and p-Si TFTs is that the p-Si devices exhibit a "kink effect" [5] in their output characteristics at high drain biases. This is a consequence of minority carrier generation near to the drain at very high electric field strengths, due to impact ionization or tunneling of these carriers out of the drain contact. The presence of the minority carriers increases the channel conductance resulting in an increase in drain current with drain voltage when the device is saturated.   Also included in our

numerical model is the velocity saturation of carriers in the channel at high electric fields.
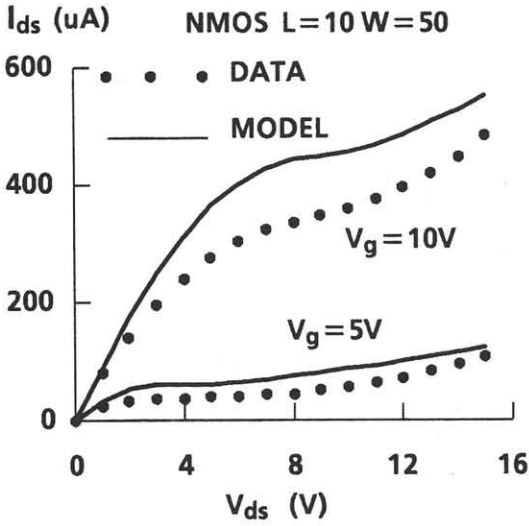
I_{ds} (uA)   NMOS L=10 W=50

Fig. 7 Computed and experimental output characteristics for NMOS p-Si TFTs, showing kink effect

In Figures 7 and 8 we show good agreement between our model and experimental output data for both NMOS and PMOS devices. The
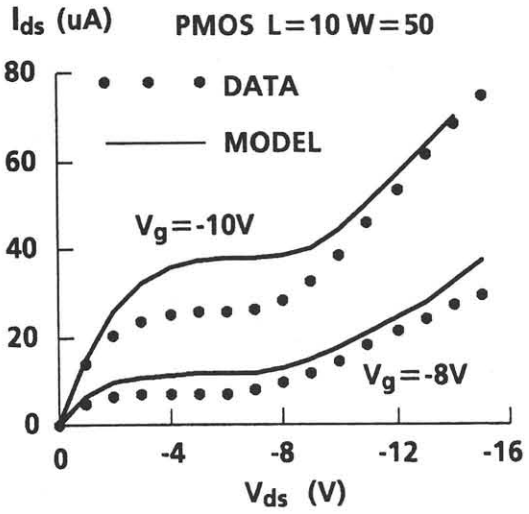
I_{ds} (uA)   PMOS L=10 W=50

Fig. 8 Computed and experimental output characteristics for PMOS p-Si TFTs, showing kink effect

expressions used to calculate the electron-hole generation, G, under high electric field in the source-drain direction, E_x, are given by

$$G = V_{sat} \ (n \, G_n + p \, G_p) \qquad (1)$$

where n and p are the free electron and hole densities, V_{sat} the saturation velocity (assumed equal for both carriers) and

$$G_n = K_n \exp (- (b_n / E_x)^{0.6})$$

$$G_p = K_p \exp (- (b_p / E_x))$$

where $b_n = 1.2 \times 10^7$ and $b_p = 3.33 \times 10^6$ V/cm. Thus we see that our effective medium model is a useful approach to predict the performance of polysilicon TFTs.

In conclusion we have shown the results of a two-dimensional numerical device simulator specifically designed to model amorphous and polycrystalline silicon TFTs where the defects or grain boundaries are assumed to be spatially uniform. Our model is in good agreement with experimental data and also predicts the "kink effect" seen in the output data for NMOS and PMOS polysilicon TFTs.

4.   REFERENCES

1) M. Hack, J.G. Shaw and M. Shur, Mat. Res. Soc. Symp. Proc. vol. 118 p. 207 (1988)

2) M. Shur and M. Hack, J. Appl. Phys. 55, 3831 (1984)

3) H. C. Tuan, Mat. Res. Soc. Symp. Proc. vol. 70 p. 651 (1986)

4) P. S. Lin, J.Y. Guo, and C.Y. Wu, IEEE Trans. Electron Devices 37, 666 (1990)

5) A.G. Lewis, T.Y. Huang, R.H. Bruce, M. Koyanagi, A. Chiang and I. Wei Wu, Technical Digest IEDM p. 264 (1988)