Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 1003-1006

S-E-17

Two-Dimensional Device Simulation for Poly-Silicon Thin-Film Transistor

So YAMADA,* Shin YOKOYAMA, and Mitsumasa KOYANAGI

Research Center for Integrated Systems,
Hiroshima University
Shitami, Saijo-cho, Higashi-Hiroshima 724, Japan

An accurate device simulator for polycrystalline-silicon thin-film transistors is developed. In this simulator, the influences of grain-boundaries (GBs) are incorporated into the mobility model, and the basic semiconductor equations are solved combining with the carrier generation/recombination model.

As a result, it becomes possible to quantitatively analyze the influence of the GBs on the kink effect and the avalanche breakdown phenomenon, and the influences of the GB trap density and the grain size on the device characteristics.

1. INTRODUCTION

Recently, the poly-Si TFT (polycrystalline-silicon thin-film transistor) has attracted a strong attention for the large-area device applications and has been intensively investigated. However, the operation mechanism of poly-Si TFT is very complicated and is still not fully understood because the poly-Si TFT includes many GBs (grain-boundaries) inside the device unlike the conventional single-crystal silicon MOS transistors or the SOI transistors. Consequently, there exist more difficulties in optimizing the poly-Si TFT structures and parameters for the device design. Therefore, it is very valuable to develop the two-dimensional device simulator for the poly-Si TFT in the view point of investigating the operation mechanisms and mitigating the difficulties in the device design.

Only a few works of the two-dimensional device simulator for the poly-Si TFT have been reported so far. In addition, even the poly-Si TFT simulators reported so far are not sufficient in terms of the validity of the physical model, the calculation time, and the calculated operation region. Particularly, they can not analyze the relation between the GBs and the kink effect or the increased off-current, which are very important in the high electric-field region.

We have developed a new two-dimensional device simulator for the poly-Si TFT that can easily analyze these phenomena. In our poly-Si TFT simulator, the influence of the GBs is incorporated into the mobility model combined with the generation/recombination model which consists of avalanche, S.R.H., and Auger processes. By using this simulator, we can accurately analyze the device characteristics of poly-Si TFTs in the wide bias range including the kink region and the avalanche breakdown region under the various device conditions.

2. SIMULATION METHOD

To simulate the device characteristics of the poly-Si TFT, it is necessary to incorporate the influence of the GBs into the simulator. Guerrieri et al.[1] carried out a two-dimensional simulation by treating the GBs as the generation/recombination centers. However, this method is not suited for the practical use since the basic semiconductor equations must be solved even in the GB region and consequently the calculation time is significantly increased.

---

* Now on leave from Electronic Imaging and Devices Research Laboratory, Fuji Xerox Co., Ltd.

For the practical and accurate simulation, we incorporate the influences of the GBs into the mobility model according to the method described below.

(1) In the poly-Si, both electron and hole mobilities are considerably smaller compared with those in the single-crystal silicon. This is because the GB forms the potential barriers against both electron and hole transport by trapping electrons and holes. Then, we express the GBs as the amphoteric carrier trapping centers, which consist of the acceptor-like trapping center for the electron and the donor-like trapping center for the hole. These trapping centers are assumed to be uniformly distributed on the GBs. The areal density and the energy level of the trapping centers are denoted as N_{tA} and $E_i + e_{tA}$ for the acceptor-like one and N_{tD} and $E_i + e_{tD}$ for the donor-like one, respectively. E_i is the intrinsic Fermi level.

(2) By using the model proposed by Lu, et al.,[2] we calculate the GB potential barrier height V_B and the GB depletion width W_{gb} from the trapped carrier areal density on the GBs, which is calculated by considering the band-bending owing to the trapped carriers, the Fermi-Dirac statistics, and the GB depletion approximation. Here, we assume that the potential barrier is formed for the electron transport if $n > p$ (n is the electron concentration and p is the hole concentration) and is for the hole transport if $n < p$.

(3) We assume the thermionic emission over the potential barrier as the carrier transport mechanism in the GB depletion region. The electron current density J_{gb} over the GB potential barrier V_B is expressed as,

$$J_{gb} = qn\sqrt{kT/2m^*\pi}exp(-\frac{qV_B}{kT}) \cdot 2sinh(\frac{qV_{gb}}{2kT}), \quad (2-1)$$

where m^* is the effective mass of electron and V_{gb} is the applied voltage to the GB depletion region.

However, since the thermionic emission theory is based on the assumption that the barrier height is sufficiently larger than kT/q so that the drift current is neglected, the calculated current density is not correct if the barrier is very low. Then, we multiply the current density J_{gb} by the V_B dependent correction factor as follows:

$$f(V_B) = 1 + \frac{\alpha}{V_B + V_B^0} \quad (2-2)$$

where V_B^0 is a fitting parameter and we take $V_B^0 = 0.1 \times (kT/q)$. The α is determined so as to

$$J_{gb} \times f(V_B = 0) = qn\mu_c V_{gb}/W_{gb}, \quad (2-3)$$

where μ_c is the mobility inside the grain. Equation (2-3) means that the current density is fully described by the drift model when the barrier is not formed.

(4) When the GB depletion width W_{gb} is smaller than the grain size L_{grain}, the voltage drop V_a in one grain is divided into V_{gb} (GB depletion region) and V_c (inside the grain), as shown in Fig.1. By considering the current continuity condition between the GB depletion region (J_{gb}) and the region inside the grain (J_c), we can simultaneously calculate V_{gb}, V_c, J_{gb}, and J_c. The effective mobility μ_{eff} is obtained from the following equation using these calculated values.

$$J_{gb} = J_c \equiv qn\mu_{eff}V_a/L_{grain}. \quad (2-4)$$

Inside the grain, the mobility model proposed by Yamaguchi[3] is used to calculate the current density.

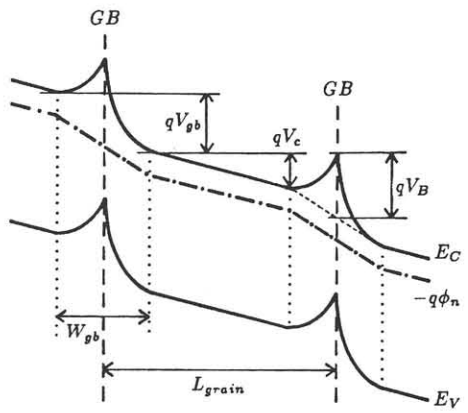

Fig. 1. Energy-band diagram of poly-Si TFT along the channel.

The Poisson's equation and the electron/hole current continuity equations are iteratively solved by the Gummel's method, employing the mobility calculated by the method described above and combining it with the generation/recombination model which consists of avalanche, S.R.H., and Auger processes.

3. $I_D - V_D$ CHARACTERISTICS

We calculated the $I_D - V_D$ characteristics for the long-channel poly-Si TFT of which the cross-sectional structure is shown in Fig. 2. Grain size $L_{grain} = 1000$Å, GB trap density $N_{tA} = N_{tD} = N_t = 1 \times 10^{12} cm^{-2}$, trap level $e_{tA} = e_{tD} = 0$ (mid-gap), and the substrate poly-Si impurity concentration $N_A = 1 \times 10^{14} cm^{-3}$ are assumed. Figure 3 shows the simulation results where the current-voltage characteristics of poly-Si TFT is compared with that of the conventional SOI transistor.

It is obvious from the figure that the current-voltage characteristics of poly-Si TFT can be calculated in the wide voltage range including the kink region and the avalanche breakdown region. The current is reduced to about 1/2 due to the influence of the GBs, when compared with the SOI transistor. In addition, the breakdown voltage is increased and the kink region is clearly observed in the poly-Si TFT.

In the poly-Si TFT with $L_{grain} = 1000$Å and $N_{tA} = 1 \times 10^{12} cm^{-2}$, GB potential barrier is highest in the region where $n \approx 1 \times 10^{17} cm^{-3}$, and hence the mobility is considerably reduced even in the channel (not pinched-off) region. The reduced mobility in the channel near the drain gives rise to the less concentrated electric field near the drain. As a result, the carriers generated due to the impact ionization are reduced. Thus the breakdown voltage of the poly-Si TFT becomes larger than the SOI transistor.

For the SOI transistor, the kink region is not observed since it is hidden behind the punch-through region in the case of the low substrate impurity concentration. On the contrary, for the poly-Si TFT, the punch-through is prevented owing to the GB potential barriers. It is also the reason why the kink region is easily observed for the poly-Si TFT that the mobility of holes generated by the impact ionization is far smaller.

These differences in the current-voltage characteristics can be explained by comparing the two-dimensional distribution of the electro-static potential for the poly-Si TFT with that for the SOI transistor. As shown in Fig. 4, in the poly-Si TFT, equi-potential lines are less spread toward the source and more gradually approach the drain due to the mobility change along the channel.

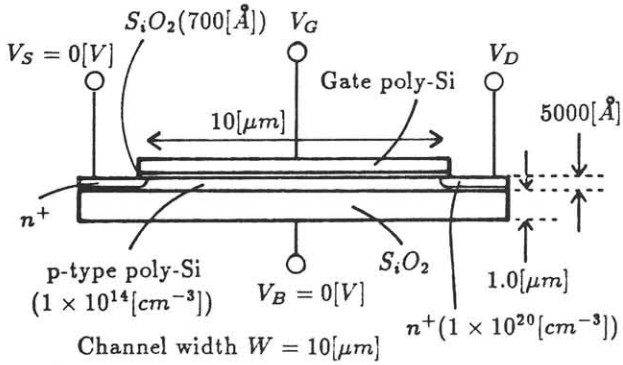

Fig. 2. Cross sectional view of poly-Si TFT.

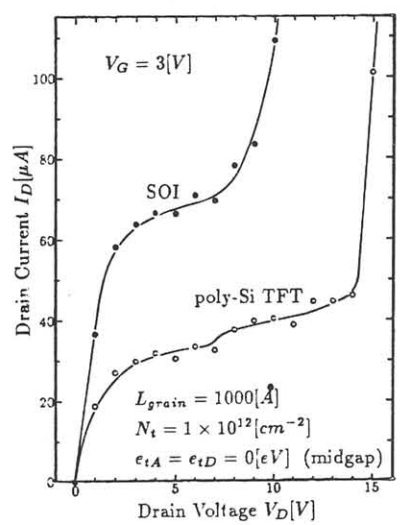

Fig. 3. Calculated $I_D - V_D$ characteristics for poly-Si TFT and for conventional SOI transistor.

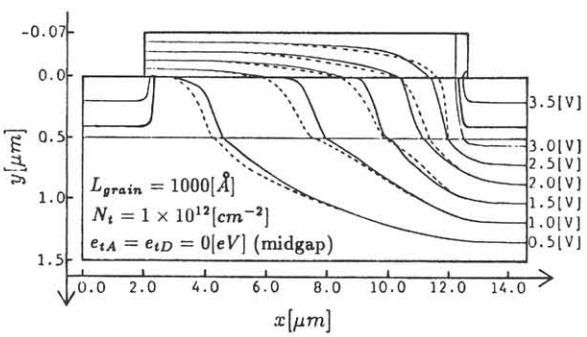

Fig. 4. Contour map of electrostatic potential ψ at $V_G = V_D = 3[V]$ for poly-Si TFT (solid line) and for SOI transistor (broken line).

4. $I_D - V_G$ CHARACTERISTICS AND FIELD EFFECT MOBILITY

Figure 5 shows the calculated $I_D - V_G$ characteristics at $V_D = 0.1V$ for the poly-Si TFT with the gate length L_{grain} of $2\mu m$ and the substrate impurity concentration N_A of $1 \times 10^{15} cm^{-3}$. In this figure, GB trap density $N_{tA} = N_{tD} = N_t$ is changed as the parameter and the grain size L_{grain} is fixed at 1000Å. N_t is the trap density per unit area at the GB which is not always equal to the effective trap density derived from the $I-V$ characteristics.[4] As shown in this figure, the threshold voltage becomes larger and the drain current becomes smaller as the trap density is increased.

In Fig. 6, we show the gate voltage dependence of the field effect mobility μ_{FE} calculated from the $I_D - V_G$ characteristics. In the low gate voltage region, μ_{FE} is decreased as N_t is increased because the GB potential barrier becomes higher. In addition, the gate voltage where μ_{FE} becomes maximum is increased with increasing N_t, because the electron concentration required to screen the barrier should be increased. In Fig. 7, we show the gate voltage dependence of μ_{FE}, varying the grain size L_{grain} as a parameter. As is obvious in the figure, μ_{FE} is decreased and the gate voltage for the maximum μ_{FE} is increased as L_{grain} is decreased.

Thus, we can accurately evaluate the influences of the GB on the poly-Si TFT characteristics by using the newly developed poly-Si TFT simulator.

5. SUMMARY

We have developed a new two-dimensional device simulator for poly-Si TFT which takes into account the influences of the GBs (grain-boundaries). By using this simulator, the simulation of the current-voltage characteristics becomes possible in the wide bias range including the kink region and the avalanche breakdown region. As a result, it becomes possible to quantitatively analyze the influence of the GBs on the kink effect and the avalanche breakdown phenomenon, and the influences of the GB trap density, the GB trap level, and the grain size on the device characteristics which were difficult to calculate by using the poly-Si TFT simulator reported so far.

REFERENCES

1) R. Guerrieri, et al.: IEEE Trans. Electron Devices **ED-33** (1986) 1201.

2) N. C. -C. Lu, et al.: IEEE Trans. Electron Devices **ED-30** (1983) 137.

3) K. Yamaguchi: IEEE Trans. Electron Devices **ED-30** (1983) 658.

4) S. Seki, et al.: IEEE Trans. Electron Devices **ED-35** (1988) 669.

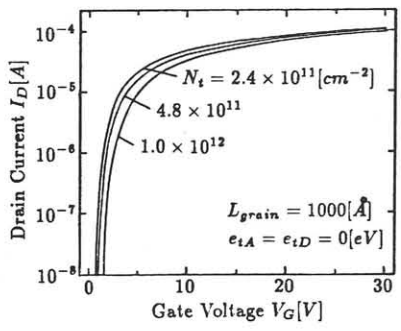

Fig. 5. Calculated $I_D - V_G$ characteristics for poly-Si TFT at $V_D = 0.1[V]$ changing GB trap density N_t as a parameter.

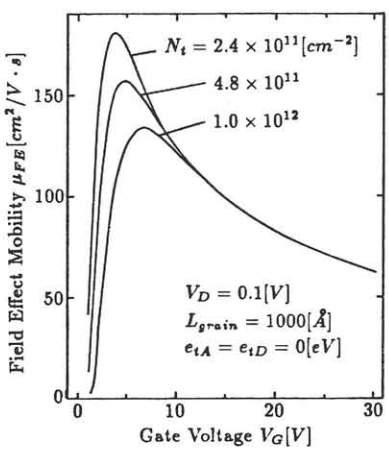

Fig. 6. Calculated $\mu_{FE} - V_G$ relations changing N_t as a parameter.

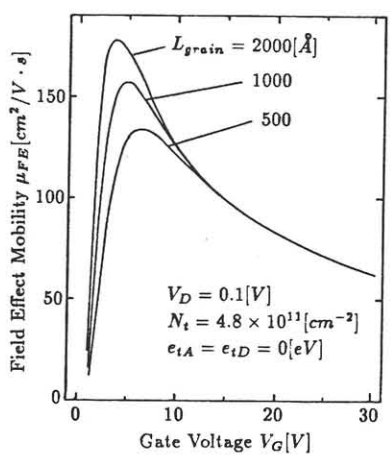

Fig. 7. Calculated $\mu_{FE} - V_G$ relations changing L_{grain} as a parameter.