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Gate Voltage Dependence of Energy Barrier Height for Inversion Carriers in Poly-Silicon TFTs

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This report describes why using the conventional thermionic emission theory is improper for the model of inversion-type poly-silicon thin film transistors. Energy barrier height, for inversion carriers in a poly-silicon thin film transistor, which is based on a previously reported new hybrid transistor model, is calculated in detail, and results are compared with measured data. The measured data can be interpreted well with the hybrid transistor model that can treat minority carrier action appropriately.

1. INTRODUCTION

Poly-silicon thin film transistor (PS-TFT) technology is now being developed intensively, in order to realize giant microelectronics with fast circuit operation capability. Since the inversion layer is used for most PS-TFT operations, inversion carrier action is very important. Conventional thermionic emission theory [1),2)] is often used to interpret the carrier action. However, the theory is not valid for minority carrier (= inversion carrier), only for majority carrier. In this report, the reason why the conventional thermionic emission theory is inadequate for inversion carriers is first clarified. Then, using a previously reported new hybrid transistor model [3)] that is able to describe PS-TFT inversion carrier action, energy barrier height for inversion carriers is calculated in detail, as an example, and results are compared with measured data.

2. LIMITATION IN CONVENTIONAL THERMIONIC EMISSION THEORY

Seto [1)] and Levinson [2)] reported that an energy barrier was created at poly-silicon grain boundary in PS-TFT, and that poly-silicon electric conduction was dominated by the thermionic emission process over the energy barrier. This model may be reasonable for determining the conduction for poly-silicon layer itself. Figure (1) shows (a) model for poly-silicon grain, (b) charge distribution along grain and (c) energy band diagram in conventional thermionic emission theory. In Fig. (1), n-type poly-silicon is depicted as an example. Majority carriers (free carriers) are electrons, and externally introduced impurity is the donor in this case (N_d:donor density). Free electrons are trapped at grain boundary, and an electric field, created by the trapped electrons, depletes free electrons near the grain boundary. Donor impurities near the grain boundary are then ionized positive. Potential distribution over the grain boundary was calculated, solving Poisson's equation with this charge distribution. Therefore, the potential barrier origin is formed by the negative majority carriers, electrons, and the ionized positive impurities, donors, in n-type poly-silicon. This theory may be used to interpret PS-TFT leak current as reported. Levinson extended the theory to accumulation mode PS-TFT [2)]. He assumed that free carrier number was the sum of introduced impurities and charges accumulated by gate voltage application. He also assumed that the ionized impurity density was modulated by the free carrier number. Under these assumptions, he reported that potential barrier height at a gate voltage could be calculated from gradient of [drain current/gate voltage] vs [1/gate voltage] plot, and that the trap state density for poly-silicon could be estimated from the barrier height. This technique has often been used in

order to evaluate poly-silicon quality. His last assumption, however, is not considered proper, because impurity density cannot be modulated by accumulation/inversion charges. In addition, since poly-silicon with no impurity in the transistor channel region is commonly used, no potential barrier can be built at a grain boundary, according to his theory.

As a result of the above consideration, the conventional thermionic emission theory cannot be used to interpret PS-TFT characteristics in subthreshold and strong inversion.

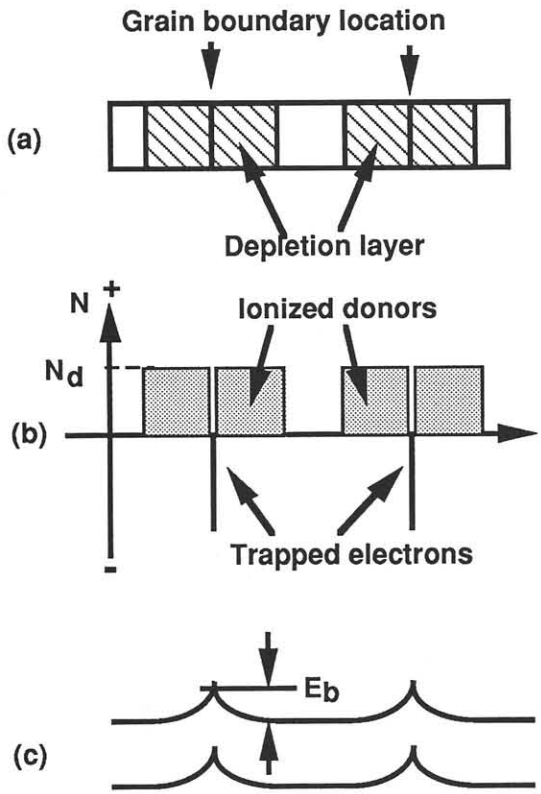

Fig. (1) Conventional thermionic emission theory diagrams. (a) Model for poly-silicon grain. (b) Charge distribution along grain. (c) Energy band diagram. E_b is energy barrier height.

3. HYBRID PS-TFT MODEL

The author has previously reported on a new hybrid PS-TFT model, that can interpret minority carrier action appropriately. [3] Figure (2) shows a PS-TFT structure, used in the hybrid PS-TFT model. Poly-silicon is divided into two regions [Regions (a) and (b)], and grain boundary regions [Region (b)] with bulk trap states intersect the silicon /silicon dioxide interface at right angles in the model. The model consists of a conventional transistor in single crystal regions in each poly-silicon grain and a newly modeled transistor in grain boundary regions, in which new model surface potential (Ψ_S [V]) is associated with a bulk trap state density (K [$V^{-1}cm^{-3}$]) in grain boundary regions. Equation (1) shows 1-dimensional Poisson's equation, used in order to incorporate effects of bulk trap state density. [3]

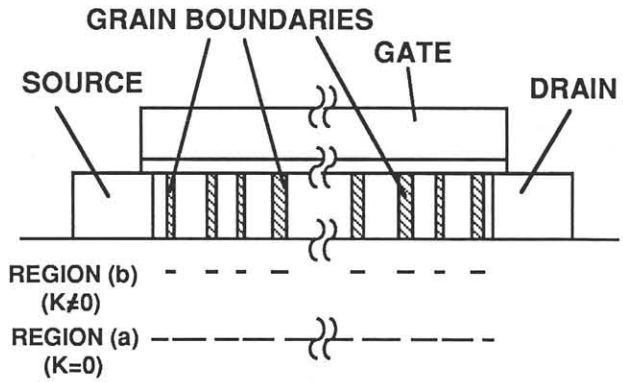

Fig. (2) Hybrid poly-silicon thin film transistor model. (a) Single crystal region in poly-silicon grains (Region (a)). (b) Grain boundary region (Region (b)). K is bulk trap density.

$$\frac{d^2\Psi}{dx^2} = -\frac{q}{\varepsilon\varepsilon_0}\left(N_d - N_a - K\Psi + p - n\right) \quad \cdots (1)$$

where the x coordinate is set perpendicular to the poly-silicon/gate oxide interface, Ψ [V]= potential, q [C] = electron charge, ε_0 [F cm^{-1}] = permittivity in free space, ε = relative permittivity in silicon, p [cm^{-3}] = hole density and n [cm^{-3}] = electron density. It is assumed that neutral bulk traps are uniformly distributed within the band gap in a poly-silicon grain boundary, and that the number of charged states is proportional to potential Ψ at any point.

Solving Eq. (1), the relation between gate voltage (V_g [V]) and Ψ_S for the newly modeled transistor can be written as follows: [3]

$$V_g = \frac{1}{C_i}\cdot\sqrt{\frac{2q\varepsilon\varepsilon_0 p_{p0}}{\beta}} \times \sqrt{\exp(-\beta\Psi_s) + \beta\Psi_s - 1 + \frac{n_{p0}}{p_{p0}}\left(\exp(\beta\Psi_s) - \beta\Psi_s - 1\right) + \frac{\beta K}{2\,p_{p0}}\Psi_s^2} + \Psi_s + V_{fb} \quad \cdots (2)$$

where C_i [F cm^{-2}] = gate capacitance, p_{p0} [cm^{-3}] = hole density in p-type silicon at thermal equilibrium, n_{p0} [cm^{-3}] = electron density in p-type silicon at thermal equilibrium, β = q/kT, k [eV K^{-1}] = Boltzmann's constant, T [K] = absolute temperature and V_{fb} [V] = flat band voltage. Surface

potentials can be calculated for grain boundary region ($K \neq 0$) and single crystal region ($K=0$), respectively, by solving Eq. (2). Inversion carrier behavior in PS-TFT can appropriately be interpreted with the hybrid PS-TFT model, because minority carrier density can be calculated from the potential and Fermi potential.

4. CALCULATED V_g DEPENDENCE FOR E_b

Surface potential difference between the two regions acts as an energy barrier for inversion carriers in the hybrid PS-TFT. Figure (3) shows gate voltage dependence for energy barrier height (E_b [eV]) for an n-channel PS-TFT. In Fig. (3), gate S_iO_2 thickness is set to 100nm, and V_{fb} is set to -10V. Ψ_s is numerically calculated for $-10V \leq V_g \leq 20V$ in a single crystal region with $K=0$ and in grain boundary region with $K=5*10^{17}$ [$V^{-1}cm^{-3}$]. Acceptor density (N_a) is used as a parameter. The E_b value increases as V_g increases from the flat-band voltage (-10V), reaches the maximum, then decreases. V_g that gives the maximum E_b increases as N_a increases. These characteristics originate from the following phenomena: Surface potential is more easily bent by V_g, and the inversion layer is created at a lower V_g in single crystal regions than in grain boundary regions.

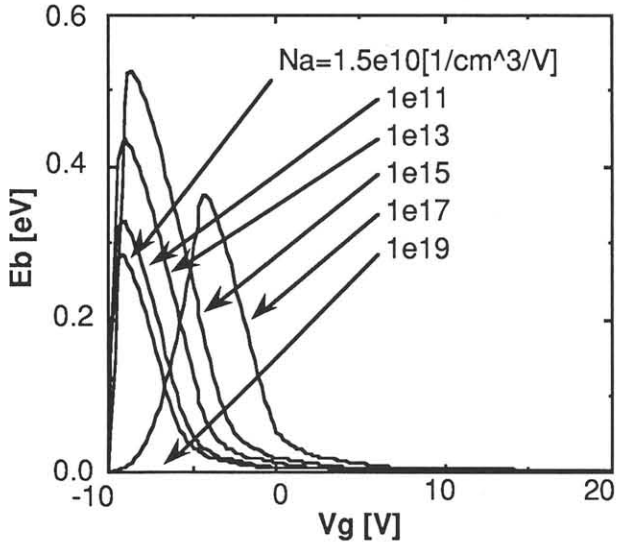

Fig. (3) Calculated E_b vs V_g characteristics using N_a ($1.5*10^{10}$, $1*10^{11}$, $1*10^{13}$, $1*10^{15}$, $1*10^{17}$, $1*10^{19}$ (cm^{-3})) as a parameter. K is set to 0 in single crystal region and $5*10^{17}$ ($V^{-1}cm^{-3}$) in grain boundary region.

Figure (4) also shows V_g dependence for E_b, using K as a parameter. N_a is set to $1.5*10^{10}$ [cm^{-3}]. The other condition is the same as in Fig. (3). Maximum E_b value increases, as K increases. Figure (5) shows maximum E_b vs log(K) plot in the K range shown in Fig. (4). It is shown that maximum E_b increases linearly to log(K). As shown in Figures (3) and (4), the hybrid PS-TFT model predicts a strong V_g dependence on E_b.

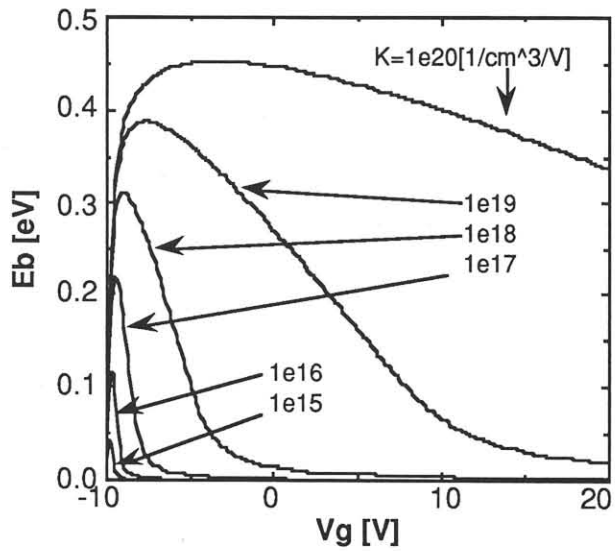

Fig. (4) Calculated E_b vs V_g characteristics using K ($1*10^{15}$, $1*10^{16}$, $1*10^{17}$, $1*10^{18}$, $1*10^{19}$, $1*10^{20}$ ($V^{-1}cm^{-3}$)) as parameter. N_a is set to $1.5*10^{10}$ (cm^{-3}).

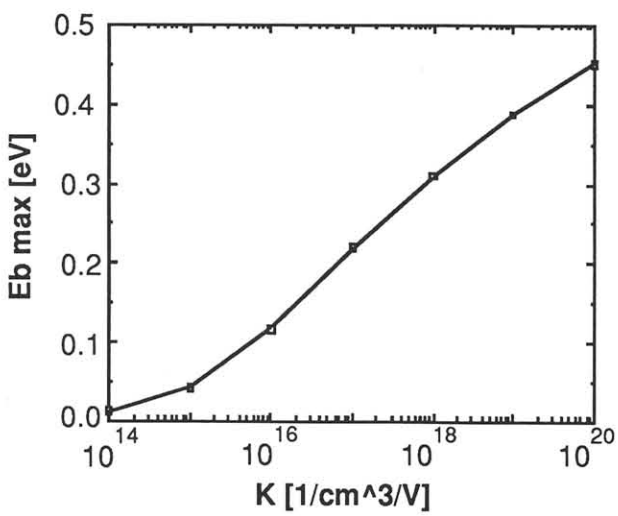

Fig. (5) Maximum E_b vs log(K)

5. MEASURED V_g DEPENDENCE OF E_b

Figure (6) shows measured V_g dependence of drain current activation energy (= E_b) for (a) n-channel PS-TFT with solid phase anneal recrystallization, (b) n-channel PS-TFT with excimer laser anneal recrystallization and (c) p-channel

PS-TFT without recrystallization procedure. Gate width to length ratio (W/L) for the measured devices is 10. About 130nm S_iO_2 is used for (a) and (b) as gate insulator. The S_iO_2 thickness for (c) is about 180nm. No dopant is introduced in channel regions for all devices.

E_b curves for (a) and (c) apparently show a strong dependence on V_g. A conventional thermionic emission model [2] is not consistent with this V_g dependence, because donors (acceptors) have to be introduced in order to build an energy barrier for electrons (holes), and because no potential barrier is built in undoped poly-silicon, as described in the above consideration. The hybrid PS-TFT model, on the other hand, can interpret the measured data very well. The V_g dependence of E_b for (a) especially matches Figs. (3) and (4) qualitatively. The p-channel PS-TFT, (c), showed higher E_b values and smaller E_b gradient when inversion is enhanced than the n-channel PS-TFT, (a). This may mean that there are many more hole traps in device (c) than electron traps in device (a). High E_b values for $-10V \leq V_g \leq 0$ may be caused by the flat-band voltage difference between the grain boundary and the single crystal region. Although the author assumed that flat band voltages were the same in the calculation for Figs. (2) and (3), it may be likely that flat band voltages differ in the two regions. In such a case, gate voltage dependence, like that for device (c), can be calculated.

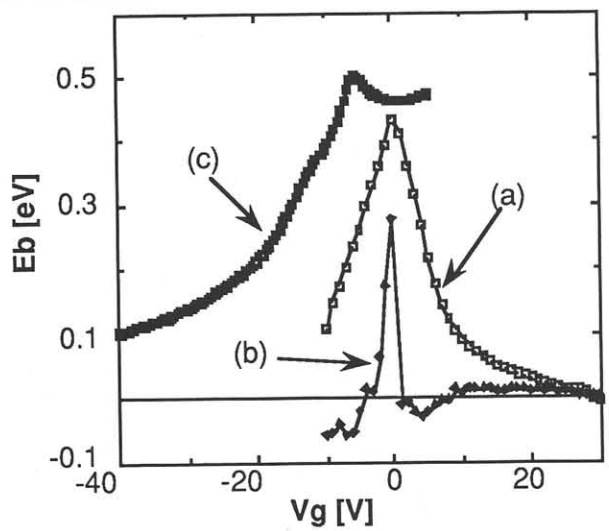

Fig. (6) Measured E_b vs V_g characteristics. (a) For n-channel PS-TFT with solid phase anneal recrystallization. (b) For n-channel PS-TFT with excimer laser anneal recrystallization. (c) For p-channel PS-TFT without recrystallization procedure.

The excimer laser annealed device (b) shows different dependence from devices (a) and (c). Since the measured drain current characteristics for (b) are as good as a single crystal MOS transistor, the measured E_b value for $V_g \leq 0$ may not show inversion carrier E_b, but leakage current. The low $|E_b|$ for $V_g > 0$ may corresponds to that for single crystal MOS transistors (a few -10 meV).

6. CONCLUSION

This report has shown why the conventional thermionic emission model is not applicable to inversion/accumulation carriers for PS-TFT. Although plausible data on energy barrier height for PS-TFT inversion/accumulation carriers have been calculated, using the model, such data do not show PS-TFT characters appropriately.

Energy barrier height has been calculated in detail, using a hybrid PS-TFT model, with which model minority carrier action can be interpreted. The calculated energy barrier height predicted a strong dependence on gate voltage. Measured data also showed a gate voltage dependence with a peak and were qualitatively interpreted well.

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REFERENCES

1) J. Y. W. Seto, J. Appl. Phys., **46**, 5247 (1975)

2) J. Levinson et al., J. Appl. Phys., **53**, 1193 (1982)

3) H. Hayama and W. I. Milne, Solid-State Electron., **33**, 279 (1990)