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# Field-Induction-Drain (FID) Poly-Si TFTs with High On/Off Current Ratio

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A field-Induction-Drain (FID) structure using a inversion layer as a drain is proposed in order to reduce the anomalous leakage current of polycrystalline-silicon thin-film transistors (poly-Si TFTs). The FID structure not only reduces the anomalous leakage current, but also maintains a high ON-current. An OFF-current of 1 pA/μm ($V_d$=10 V, $V_g$=-20 V) and an ON/OFF current ratio of $10^7$ ($V_d$=10 V) are successfully obtained. This FID poly-Si TFT is very promising for application to active-matrix LCDs.

## 1. Introduction

Polycrystalline-silicon thin film transistors (poly-Si TFTs) are expected to be used for the peripheral and active-matrix circuits in large area liquid-crystal displays (LCDs) because of their high field-effect mobility and reliability. However, conventional poly-Si TFTs have a large OFF-current ($I_{OFF}$), which is unsuitable for active-matrix applications.

In order to reduce the $I_{OFF}$, several studies to reduce electric field at a drain junction have been performed[1)2)]. However, problems such as an insufficient ON-current still remain.

In this paper, we propose a new $I_{OFF}$ reduction structure, Field-Induction-Drain (FID), e.g., an inversion layer induced by the electric field is used as a drain. The characteristics of this FID TFT are also presented, and the related mechanisms are discussed.

## 2. FID TFT structure

The fundamental structure of an n-channel FID TFT is shown in Fig. 1. The main feature of the FID TFT is that a inversion layer formed under the sub-gate is used as a drain. The formation of the inversion layer is controlled by the sub-gate voltage (Vs).

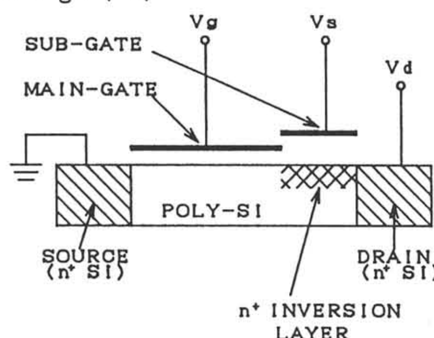



Fig.1 Fundamental FID TFT structure.

A cross-sectional view of a fabricated FID TFT is shown in Fig. 2. Both source and drain are phosphorous-doped poly-Si films. The active layer is a poly-Si film formed by solid-phase crystallization of an LPCVD a-Si film[3)]. The gate insulator is a sputtered $SiO_2$ film (100 nm) [4)]. The interlayer insulator is a sputtered $SiO_2$ film (400 nm) or a plasma CVD $SiN_x$ film (400 nm). The main-gate is a phosphorous-doped poly-Si film. The sub-gate was formed by an aluminum on the interlayer insulator.

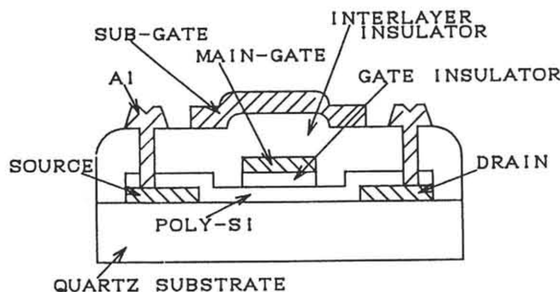



Fig.2 Cross-sectional view of fabricated FID TFT. (W/L=10 µm/10 µm)

Sub-gate length $L_s$, main-gate length L, and gate width W, are 2 µm, 10µm and 10 µm, respectively.

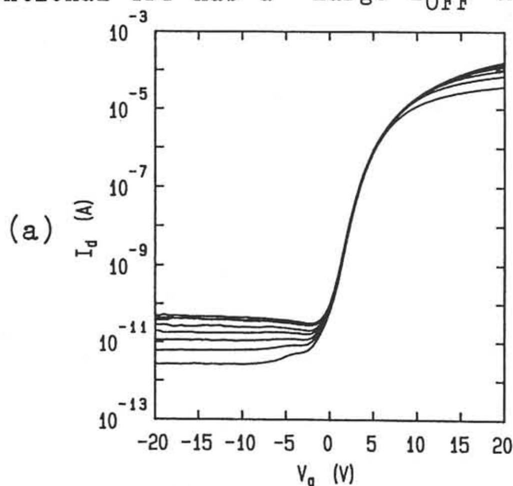
The basic characteristics of the FID TFT were estimated using a four terminal device in which the sub-gate was one terminal. For application purpose, the characteristics of a FID TFT in which the sub-gate was connected to a drain were also investigated.

Both the temperature (20 °C- 175 °C) and drain voltage dependencies of $I_{OFF}$ were measured to clarify the FID junction characteristics.

### 3.FID TFT characteristics

The $I_d$-$V_g$ characteristics of an n-channel FID TFT at $V_s$=60 V are shown in Fig. 3(a). For comparison, those of a conventional TFT are shown in Fig. 3(b). The conventional TFT has a large $I_{OFF}$ that increases as negative gate voltage and positive drain voltage increase. On the other hand, the FID TFT has a sufficiently low $I_{OFF}$ that remains almost constant regardless of gate voltage. $I_{OFF}$ is as low as 1 pA/µm ($V_d$=10 V, $V_g$=-20 V), and $I_{ON}$ is sufficiently high (field effect mobility : 35 $cm^2$/Vsec). Thus, an ON/OFF current ratio of $10^7$ is achieved at $V_d$=10 V.

However, a sub-gate voltage of 60 V is too high for the application of an FID TFT. It is necessary to obtain a low resistivity inversion layer at low sub-gate voltage. Therefore, a $SiN_x$ interlayer deposited by plasma CVD is used to reduce the threshold voltage in a sub-gate region. The $I_d$-$V_g$ characteristics of a conventional TFT with a $SiN_x$ gate insulator are shown in Fig. 4. This TFT has deep-depletion characteristics (threshold voltage: -6 V). The $V_s$ dependence of $I_{ON}$ and $I_{OFF}$ for an FID TFT with an $SiO_2$ interlayer and an FID TFT with an $SiN_x$ interlayer are shown in Fig. 5 (a). The $I_d$-$V_g$ characteristics of a three terminal FID TFT with its sub-gate connected to drain ($V_d$=10 V) are shown in Fig. 5(b). By using a $SiN_x$ interlayer, a high $I_{ON}$ and a low $I_{OFF}$ can be obtained even at a low sub-gate voltage. Furthermore, for the three terminal device, $I_{ON}$ was successfully improved while maintaining a sufficiently

(a) 

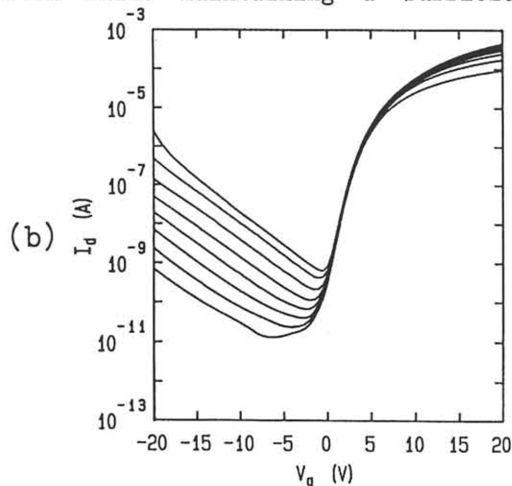

(b) 


Fig.3 $I_d$-$V_g$ characteristics of n-channel FID TFT($V_s$=60 V) (a) and conventional TFT (b). ($V_d$=2.5 V- 20 V, 2.5 V step)

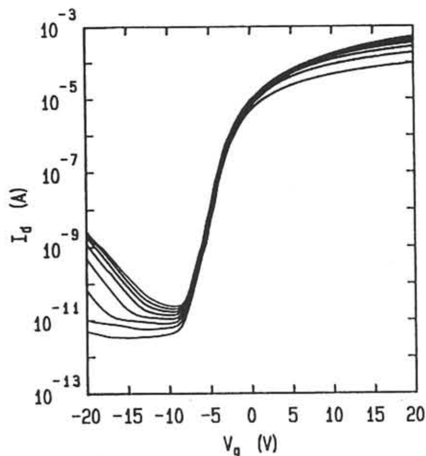
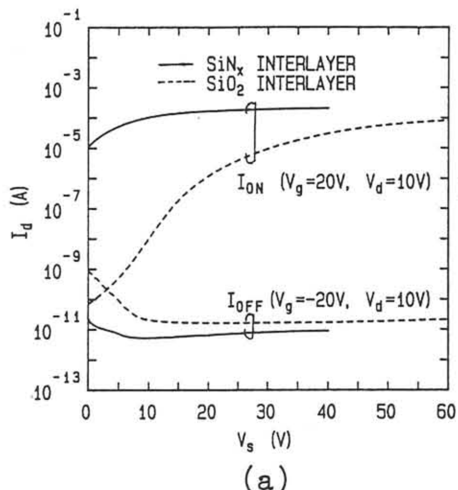



Fig.4 $I_d$-$V_g$ characteristics of conventional TFT with $SiN_x$ gate insulator. ($V_d$=2.5 V- 20 V, 2.5 V step)



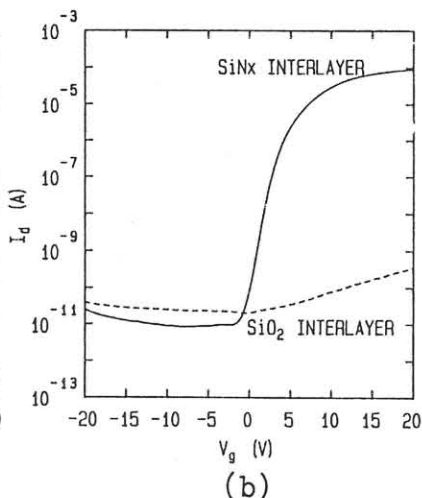



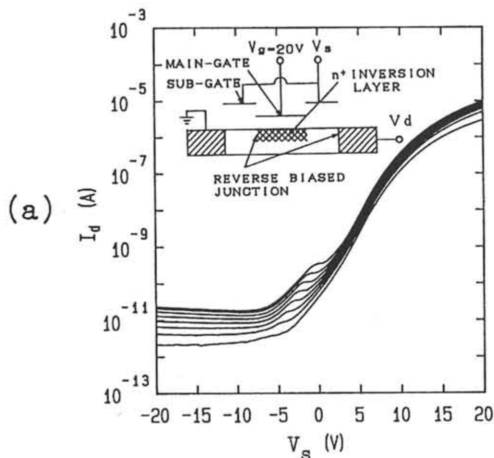

Fig.5 (a)$V_s$ dependence of $I_{ON}$ and $I_{OFF}$ in FID TFT with $SiO_2$ interlayer or $SiN_x$ interlayer. (b)$I_d$-$V_g$ characteristics of FID TFT with sub-gate is connected to drain ($V_d$=10 V).

low $I_{OFF}$. This means that a simple circuit configuration is applicable to the FID TFT.

## 4.FID junction characteristics

To clarify the reason why a low $I_{OFF}$ is obtained in the FID TFT, FID junction characteristics are investigated. The $I_d$-$V_s$ characteristics of the FID TFT at $V_g$=20 V are shown in Fig. 6(a). Under this condition, an inversion layer is formed under the main-gate, as shown in inset in Fig. 6 (a). The $I_d$-$V_s$ characteristics of a conventional TFT with a sub-gate only are shown in Fig. 6(b). These results show that the inversion layer under the main-gate also reduces $I_{OFF}$. In the FID TFT with an inversion layer under the main-gate, two reverse biased junctions are formed. The conventional drain junction is shown to be leaky by Fig. 6 (b). Therefore, the low $I_{OFF}$ of the FID TFT is due to the good junction characteristics between the channel and the induced inversion layer.

The $V_d$ dependence of $I_{OFF}$ of the FID TFT ($V_s$=60 V) and a conventional TFT are shown in Fig. 7. $I_{OFF}$ was measured at $V_g$= -20 V. In the conventional TFT, $I_{OFF}$ increase is accelerated by the drain voltage. On the other hand, the $I_{OFF}$ of the FID TFT increases proportional to $V_d^x$ (x=0.5-1),



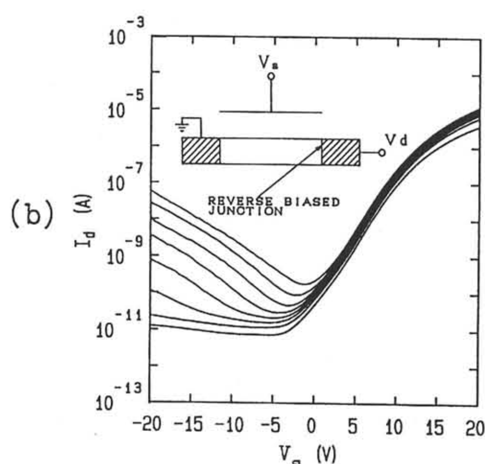




Fig.6 $I_d$-$V_s$ characteristics of FID TFT at $V_g$=20 V (a) and conventional TFT with sub-gate only (b). ($V_d$=2.5 V- 20 V, 2.5 V step)

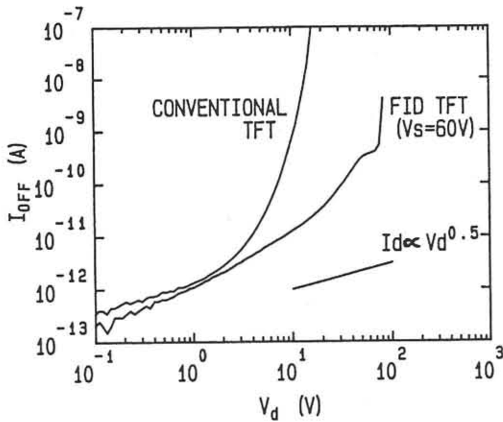



Fig.7 $V_d$ dependence of $I_{OFF}$ in FID TFT ($V_s$=60 V) and conventional TFT. ($I_{OFF}$:$V_g$=-20 V)

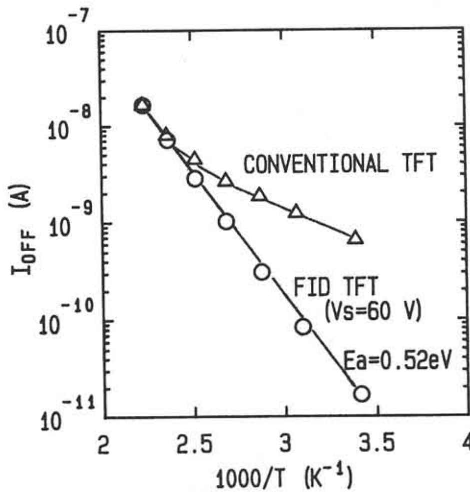



Fig.8 Temperature dependence of $I_{OFF}$ in FID TFT ($V_s$=60 V) and conventional TFT. ($I_{OFF}$:$V_g$=-20 V,$V_d$=10 V)

and exhibits abrupt breakdown characteristics at about $V_d$=70 V. The temperature dependence of the $I_{OFF}$ of the FID TFT ($V_s$=60 V) and a conventional TFT are shown in Fig. 8. $I_{OFF}$ was measured at $V_g$=-20 V, $V_d$=10 V. The $I_{OFF}$ of the conventional TFT shows a weak temperature dependence due to field emission current[5]. On the other hand, the FID TFT has a strong temperature dependence at an activation energy, $E_a$, of 0.52 eV. These results suggest that the $I_{OFF}$ of the FID TFT is only dominated by generation-recombination current, not field-emission current.

The improvement in the drain junction characteristic of the FID TFT over the conventional TFT is considered to be due to a reduction of the trap density at the drain junction. The junction in the FID TFT is free from an increased defects caused by the doping process. This is considered to be the reason for the low trap density and low $I_{OFF}$.

## 5.Conclusion

An FID TFT using an inversion layer as a drain is proposed. An $I_{OFF}$ of 1 pA/μm ($V_d$=10 V, $V_g$=-20 V), and an ON/OFF current ratio of $10^7$ are successfully obtained by the FID TFT. Furthermore, reducing the threshold voltage of the sub-gate region allows a simple circuit configuration to be applied to these TFTs. Moreover, measurement of the junction characteristics proved that the $I_{OFF}$ of the FID TFT is only dominated by generation-recombination current, not the field-emission current. These results indicate that FID TFTs can improve the active-matrix circuit characteristics of LCDs.

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## References

1) K. Tanaka, H. Arai, S. Kohda; IEEE Electron Device Letters, 9 (1988) 23.

2) T. Chuang, I. Wu, T. Huang, A. Chiang; SID '90, digest, (1990) 508.

3) K. Nakazawa, T. Tanaka, S. Suyama, K. Kato and S. Kohda; SID '90, Digest, (1990) 311.

4) S. Suyama, A. Okamoto and T. Serikawa; J. Electrochem. Soc., 134 (1987) 2260

5) J. Fossum, A. Ortiz-conde, H. Shichijo, S. Banerjee; IEEE Trans. Electron Devices, 41 (1985) 1878.