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Active Devices for Large Area Electronics

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A comparison is made between the properties of basic TFT and diode devices fabricated using a-Si and low temperature polysilicon technology. It is shown that all device properties are degraded by the high concentration of defect centres in these materials relative to single crystal silicon devices but useful devices can be made provided electron and hole concentrations remain low during operation. Polysilicon is less sensitive to meta-stable defect creation but the short generation time and narrower band gap leads to much greater leakage currents compared with a-Si.

1. INTRODUCTION

The ability to make active semiconductor devices over large areas on inexpensive substrates opens up a wide range of possibilities for new electronic devices[1] and inexpensive circuits. Silicon based materials systems incorporating amorphous silicon or polysilicon are particularly interesting because of their ease of fabrication and the abundance of raw materials. When considering what active devices will be needed for large area electronics one naturally turns to device concepts closely analogous to those that have been used so successfully in single crystal silicon. In this paper, we compare the properties of the main building blocks of electronic circuits in these silicon based technologies, namely transistors and diodes. In many respects these disordered materials are inferior to single crystal silicon and their range of applicability is limited but there are also some very real advantages which make them superior even to single crystal silicon for some applications. The major problem that has to be understood and allowed for is that of stability. In general, single crystal devices are stable over wide ranges of electric field, current density and temperature whilst devices used for large area electronics are not, for one reason or another, and measures have to be taken to minimise or compensate for these effects. This paper outlines the properties of the basic bipolar and unipolar devices; no mention will be made of the novel device structures[2,3] or exciting phenomena[4] that are currently being explored, based on these thin film technologies.

2. GENERAL CONSIDERATIONS

A comparison of the most important device and material properties in poly and amorphous silicon (Table 1) shows that we are dealing with devices having very different properties compared with single crystal silicon. In particular the large densities of generation/recombination centres lead to very much shorter recombination lifetimes and diffusion lengths.

Table 1

						F.E.T.		p-i-n	
	E_G (eV)	E_{BR} V/cm	τ_G sec.	τ_R sec.	N_T $cm^{-3}eV^{-1}$	μ_{FE} $cm^2V^{-1}sec^{-1}$	Leakage/ Channel Width A/μm	n	J_S A/cm^2
C-Si	1.15	$2x10^5$	$10^{-4} \rightarrow 10^{-3}$	$\approx 10^{-4}$	$\approx 10^{10}$	≈ 600	$\approx 5x10^{-16}$	-	$\approx 10^{-9}$
a-Si:H	1.8	$>1x10^6$	-	$\approx 5x10^{-7}$	$10^{16} \rightarrow 10^{17}$	0.5 → 0.9	$\approx 5x10^{-16}$	1.8 (p-i-n) 1.3 (n-i-p)	$\approx 5x10^{-11}$ $\approx 1x10^{-11}$
poly-Si	1.15	$\approx 2x10^5$	$\approx 3x10^{-10}$	$\approx 1x10^{-10}$	$10^{16} \rightarrow 10^{17}$	20 → 60	$\approx 2x10^{-14}$	-	$\approx 10^{-4}$
						V_{DS} = 5 V	L = 10 μm	i thickness ≈ 0.5 μm	

The values for τ_R in polysilicon corresponds to minority carrier diffusion length of 0.1 μm which is close to the grain size, whilst in a-Si:H, τ_R is determined by trapping and recombination within a wide distribution of dangling bond and deep level states. However, the field dependence of the minority carrier diffusion length and the fact that large fields can be sustained in these materials without breakdown implies that even with low mobilities and short lifetimes, minority carriers can migrate several hundred nanometres in device structures.

3. BIPOLAR DEVICES

The short carrier recombination lifetime in both a-Si and polysilicon makes these materials unsuitable for the formation of useful bipolar transistors although it is not inconceivable that a bipolar transistor could be made in polysilicon if the grain size was similar to the base width. Bipolar p-i-n and n-i-p diodes, however, can be made with acceptable ideality factors (Table 1 and Fig. 1) and in the case of a-Si:H a leakage current lower than the best attainable in crystalline silicon can be achieved despite its short generation lifetime. This property arising from the larger band gap of a-Si:H makes it the preferred material for applications where a very low leakage is required. Polysilicon silicon, however, is never likely to achieve leakage comparable with the best in single crystal because of the preponderance of generation centres at grain boundaries. The maximum forward current density, determined by the onset of space charge limited currents in the intrinsic layer, is low in these amorphous materials ($\approx 10^{-1}$ amp.cm^{-2}) because of majority carrier trapping and very low carrier mobilities. Furthermore, the short minority carrier lifetime severely restricts the depth of conductivity modulation.

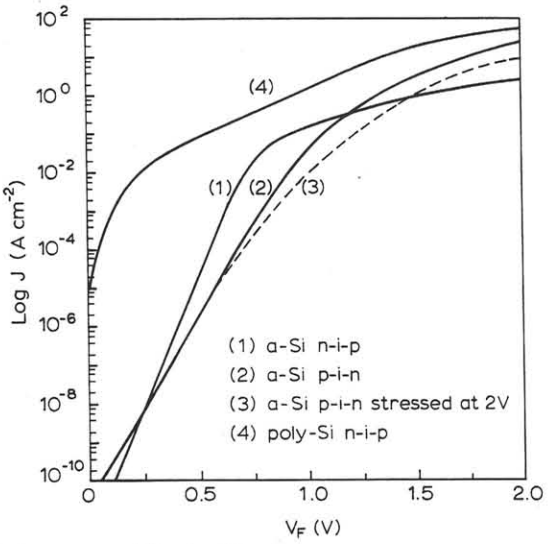

Fig. 1 Bipolar Devices

An interesting difference between a-Si p-i-n and n-i-p devices is the magnitude of the ideality factor (Table 1). This is most likely due to a difference in the distribution of generation/recombination levels in the i region and their dependence on the order of growth of the layer (p region first in p-i-n).

In polysilicon, the p-i-n characteristic shows a leakage current (J_S) many orders of magnitude higher than single crystal silicon. In the forward direction there is clear evidence of recombination current and conductivity modulation but the short lifetime ensures that effects are small with only an order of magnitude increase in conductivity compared with a non-injecting n-i-n structure (Fig. 3).

The application of current stress can increase the effective ideality factor (Fig. 1) as deep states are introduced into the i region and more electrons and holes are trapped. After prolonged current stress, the change of conductivity in the a-Si device suggests that transport becomes dominated by Poole-Frenkel emission from metastable deep levels throughout the i-layer with the concentration and distribution of these levels depending on the electron and hole concentrations in the device during operation. These effects are discussed further below.

4. UNIPOLAR DEVICES

4.1 FETs

A comparison between the common n-channel TFT structures in amorphous and poly-silicon is made in Table 1 and Fig. 2. The large density of electron traps in a-Si increases the sub-threshold slope compared with single crystal silicon and the density of localised tail states controls the mobility. In poly-silicon where these traps and states occur mainly at grain boundaries the mobility is higher. The leakage current in the off-state is, as expected, lower in a-Si at a given drain voltage but the difference depends to some extent on channel length because in a polysilicon TFT which normally operates in inversion, the voltage is held off by the drain junction whilst in a-Si TFTs the field is dropped across the entire length between source and

drain. The difference in the leakage current of amorphous and poly TFTs designed for the same on-current is small despite a very large difference in leakage per unit area because only the edge of the drain junction contributes to the leakage when the drain junction penetrates to the substrate boundary.

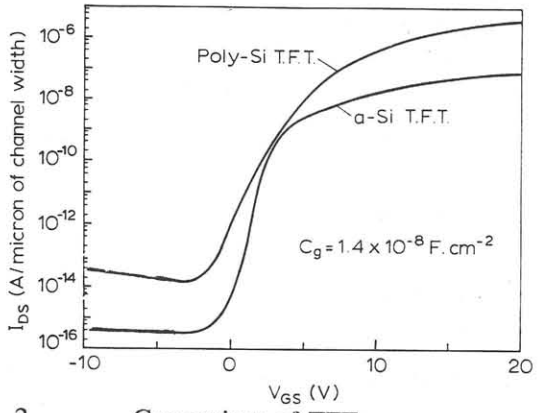

Fig. 2 Comparison of TFTs

Under current and voltage stress, device stability is determined by charge trapping in the gate insulator and the creation of metastable defects in the silicon layer[5]. The former is expected to the more pronounced in polysilicon transistors due to the large fields around the drain whilst the latter will dominate in a-Si where the density of weak bonds is higher. In practice both effects have been found in both materials[6,7,8] but the most fundamental is state creation since trapping in the insulator can be avoided by operating at low gate and drain biases.

4.2 Diodes

The current-voltage characteristics of n-type unipolar diodes are compared in Figure 3. As with

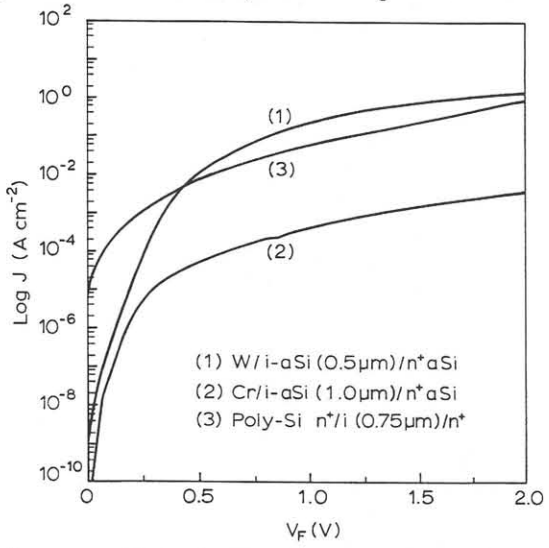

Fig. 3 Unipolar Devices

p-i-n structures the leakage current of the poly n-i-n is high and in the forward direction diode quality is very poor because of the presence of states at grain boundaries. In amorphous silicon an ideality factor of 1.2 is measured for Schottky barriers and the quality of barriers is acceptable. The current starts to be limited by the resistance of the i region, however at $\simeq 10^{-3}$ amps/cm^2; an order lower than p-i-n diodes presumably because of absence of hole injection. The behaviour of these metal-semiconductor diodes under a reverse bias and large electric fields is shown in Fig. 4 where two back to back Schottky barriers are separated by a 800 Å a-Si layer. The almost exponential increase in current when the electric field is high is consistent with thermionic-field emission of electrons through a

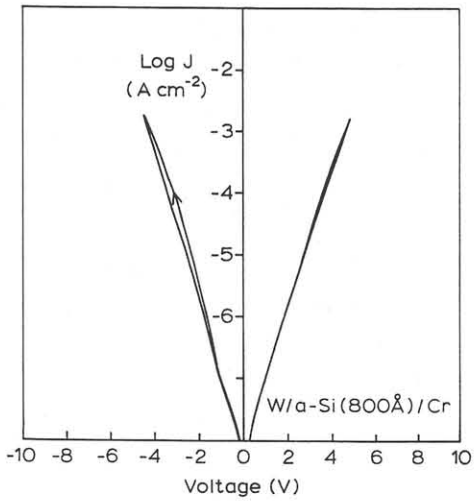

Fig. 4 Back to Back a-Si Schottky

reverse biased barrier[9]. The very high electric field in this structure and the corresponding high drift mobility of the electrons combined with the field enhanced detrapping from deep levels enables current densities exceeding 10 amps/cm^2 to be obtained without the onset of space-charge limited currents. Current stress increases the concentration of deep levels but changes are small and can be almost negligible since current densities are low.

In order to clarify why structures containing a doped contact (Fig. 1) showed a greater rate of degradation than those having a metal surface barrier, metal-i-n$^+$ structures were made. The I/V characteristics (Fig. 5) showed, as expected, that initially the current was limited by the metal contact in the reverse direction (metal -ve) and by the i region in the forward direction. Under stress in the forward direction the I/V characteristics changed much more rapidly than in a

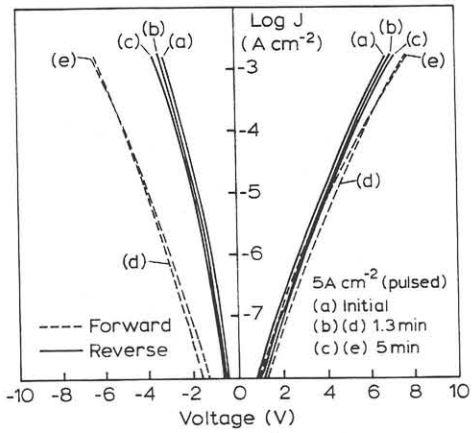

Fig. 5 I/V After Current Stress

similar device stressed in the reverse direction at the same current density. These results suggest that the rate of introduction of metastable states and the total number in steady state is related to the electron concentration in the i layer. When the n^+ i region is injecting electrons the field is low and the electron concentration high whilst when the reverse biassed Schottky is injecting the field is high and the electron concentration lower (Fig. 6). These results suggest that the rate of metastable state creation depends primarily on the electron concentration[10] and is less dependent on the magnitude of the electric field. Such behaviour is consistent with state creation in a-Si TFTs based on the defect pool model[7].

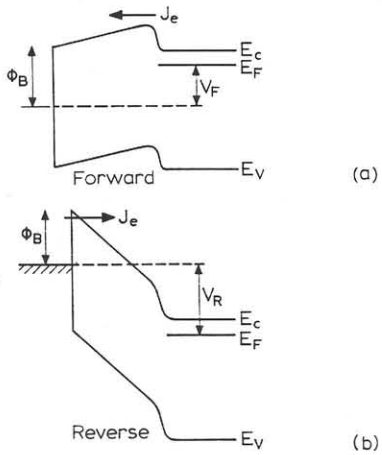

Fig. 6 Band Diagram for Metal/i/n^+

5. CONCLUSIONS

We see from the characteristics of basic device structures in amorphous and poly-silicon that the large density of centres in the band gap leads to pronounced effects on device performance compared with single crystal devices. Space charge limited currents, carrier trapping and metastable state creation can all occur at current densities orders of magnitude below those commonly used in single crystal devices. Furthermore, short minority carrier lifetimes prevent any major improvements in device performance from the use of minority carrier injection.

The wider band gap of a-Si leads to real advantages when it comes to low leakage with current densities well below the best that can be obtained in single crystal silicon. Present polysilicon devices, however, have leakage currents orders of magnitude higher than crystalline silicon because of the high concentration of deep centres at grain boundaries.

Metastable state creation is particularly important in amorphous silicon as it strives to reach a steady state equilibrium during device operation. Similar effects probably occur in polysilicon devices but to a lesser extent. The number of states formed would seem to be primarily related to the electron (or hole) concentration during device operation. At low current densities (<1 amp/cm^2) and low fields (<10^4 V.cm^{-1}) good quality, fairly stable devices can be made and a wide range of devices and circuits should be achievable using amorphous and poly silicon technologies but stability remains an issue, particularly for analogue circuits. It will be essential to resort to electronic techniques to compensate for device instability in many cases.

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7. REFERENCES

1) P.G. LeComber: Jr. Non-Crystalline Solids **115** (1989) 1.
2) M. Meunier, M. Bisson, M. Kemp: Jr. Non-Crystalline Solids **115** (1989) 108.
3) M. Yoshimoto, T. Fuyuki, H. Matsunami: Jap. J. Appl. Phys. **25**, 11 (1986) L922.
4) M.J .Rose, J. Hajto, M.J. Rose, P.G. LeComber, S.M. Gage, W.K. Choi, A.J. Snell, A.E. Owen: Jr. Non-Crystalline Solids **115** (1989) 168.
5) M.J. Powell: IEEE Trans - ED **36**, 12 (1989) 2753.
6) N.D. Young, A. Gill: Semicond. Sci. Technol. **5** (1990) 72.
7) M.J. Powell, I.D. French, J.R. Hughes: Jr. Non-Crystalline Solids **114** (1989) 642.
8) I-W. Wu, W.B. Jackson, T-Y. Huang, A.G. Lewis, A. Chiang: IEEE Trans - ED **11**, 4 (1990) 167.
9) J.M. Shannon: Solid State Electronics **19** (1976) 537.
10) M.J. Powell, C. van Berkel, J.R. Hughes: Appl. Phys. Lett. 54 (1989) 1323.