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Short-Channel Inverted Staggered a-Si:H Thin Film Transistors Fabricated by Electron-Beam Lithography

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Short-channel hydrogenated amorphous silicon thin-film transistors have been fabricated by using Electron Beam Litography with shortest channel length of .44 μm. The devices are showing field-effect mobiity around .7 cm^2/Vs independently on the channel length. This result is related to low parasitic resistance shown by our devices and attributed to the Al-diffusion in the source-drain contact regions.

1. INTRODUCTION

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) are finding increasing interest in the field of large area microelectronics[1]. In particular the application to flat-panel display is one of the most attractive and developed, although at present still two problems prevent this technology to meet the final success: stability and speed.

To increase the operation speed two basic approaches are possible: enhance the field-effect mobility and reduce the channel length. To reduce the channel length different vertical TFTs structures have been proposed [2,3] and only very recently submicrometer channel planar structure have started to be investigated [4,5].

However, from the study of conventional staggered TFTs a decrease in the field-effect mobility with the decrease of the channel length, L, is observed. This effect, generally attributed to increasing weight of the parasitic resistance over the channel resistance at small channel lengths, if not eliminated, makes non promising the philosophy of reducing L.

In the present study we investigated conventional inverted staggered TFTs down to .44 μm of channel length without finding a sensible degradation of field-effect mobility. The results are particulary relevant in view of understanding the limiting factors of device speed.

2. DEVICE FABRICATION

Inverted staggered structure TFTs are fabricated on Corning Glass 7059. First large area bottom gates are formed with 100 nm of Cr and patterned using conventional lithographic techniques. Together with the gates, alignement markers for the Electron-Beam Litography (EBL) are also defined. Next, 60 nm a-SiO_2, 70 nm a-Si:H and 30 nm n^+ a-Si:H are sequentially deposited in a radial-flow hot-wall Plasma Enhanced CVD (PECVD) reactor. The electrical properties of our a-SiO_2 are similar to those relative to thermal silicon dioxide, with breakdown fields exceeding 10 MV/cm and no significant charge injection up to fields of 5-6 MV/cm [6,7].

Deposition conditions are:

1) a-SiO_2: 2 sccm SiH_4 + 100 sccm N_2O + 100 sccm He at total pressure, p, .7 Torr, RF power density, P, 20 mW/cm^2 and substrate

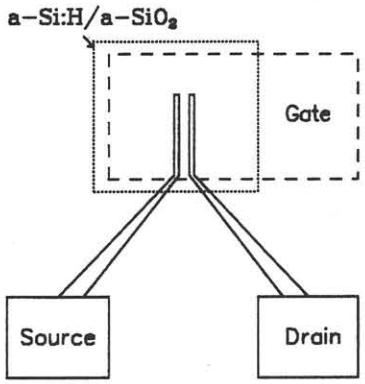

Fig.1 Layout of EBL-fabricated short-channel device.

temperature, T_s, 250 °C;

2) a-Si:H: 20 sccm SiH_4, T_s = 250 °C, P = 20 mW/cm^2 and p = .3 Torr;

3) n^+ a-Si:H: 20 sccm of 1 % PH_3 in SiH_4, T_s = 250 °C, P = 20 mW/cm^2 and p = .3 Torr.

The Electron-Beam Litography patterning was performed using a Cambridge Instruments EBMF 6.4 machine. The accelerating voltages used in the experiments were 30 and 40 KV and the probe current was 2 nA. In these conditions our machine delivers a tipical beam spot size of 70 nm. The electroresist was a commercial Polymethil-methacrilate (PMMA) spun 0.5 μm thick and developed at 20 °C in a mixture 1:1 of Isoprophyl Alcohol and Methyl-isobuty-ketone for a total time of 1 minute.

This process has been found to be suitable for defining of the required undercut resist profile (lift-off metallization technique) even for closely spaced source and drain contacts and without any proximity effect correction.

The source and drain contacts are 1 μm wide and the channel length ranges between 10 μm - .5 μm (a planar view is shown in Fig.1). To form source-drain contacts alternatively 120 nm Cr or 200 nm Al were electron-gun evaporated and lifted off using the electroresist solution. Then, a-Si:H islands are formed and the n^+ a-Si:H is etched-off the back channel by plasma etching. Finally, the devices were annealed

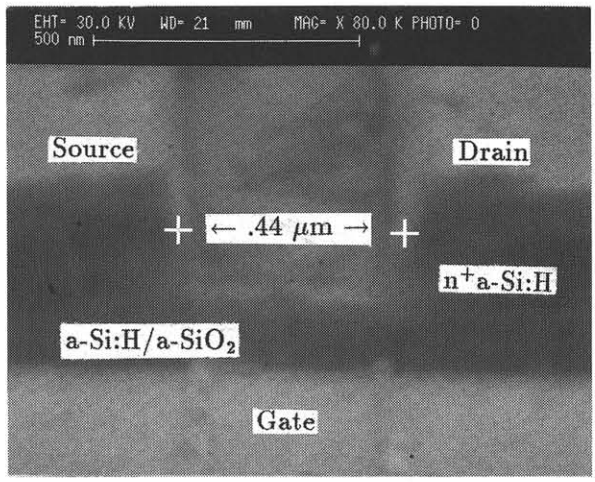

Fig.2 Cross-sectional SEM photograph for the shortest channel length.

in vacuum at 200 °C for 1 h

A cross-sectional SEM photograph for the shortest channel length, whose geometrical size is about .44 μm, is shown in Fig.2.

3. RESULTS AND DISCUSSION

Before to examine the results relative to the above mentioned devices, let us first describe the effect of reducing the channel length in conventional inverted staggered a-Si:H TFTs, fabricated by using the same materials, where however a 300 nm thick a-Si:H layer was used as active layer and 18 nm thick a-SiO_2 as gate insulator. Further fabrication details can be found in ref.6.

Figure 3 shows the effect of reducing L from 20 to 2.5 μm on the field-effect mobility, μ_{FE}, deduced from $I_d^{1/2}$ vs V_g plot of saturated characteristics. As can be seen, μ_{FE} decreases monotonically as L decreases and a possible explanation can be found in Fig.4 where $R = \frac{dV_{ds}}{dI_d}$, deduced for low V_{ds} and constant V_g, vs L is reported. If R would consist only of the channel resistance then a linear dependence with L is expected with R = 0 for L = 0 [5]. On the contrary the extrapolated value of R for L → 0 is finite and depends on V_g. This can be connected to the parasitic resistance composed by the series of Al/n^+ a-Si:H and n^+ a-Si:H/a-Si:H contact resistances plus the

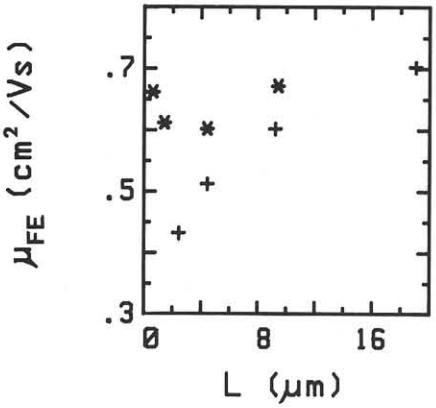

Fig.3 Field-effect mobility vs channel length for conventionally (+) and EBL (*) fabricated devices.

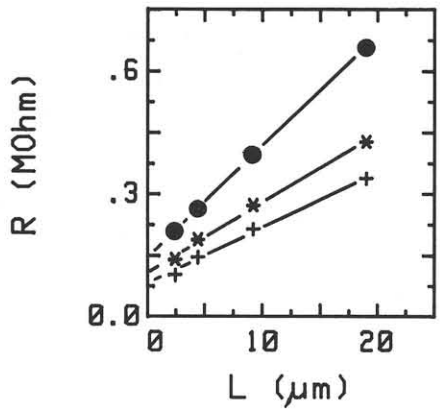

Fig.4 Resistance,R, vs channel length, L, for conventionally fabricated devices, at different gate voltages: (+) $V_g = 5$, (*) $V_g = 4$, (•) $V_g = 3$.

contribution arising from the unaccumulated a-Si:H that the electrons from the channel must traverse to reach the source and drain contacts. Space-charge limited current is usually assumed to be involved in this last region[8].

On the basis of these data, it would appear non attractive to scale down the channel length since the characteristics for low L are dominated by parasitic resistance. Busta et al.[5] reached same conclusions investigating short-channel devices, although the value of μ_{FE} quoted for their long channel devices appears somewhat too small if compared with the current a-Si:H TFTs technology, implying problably some additional problem. The data relative to our EBL-fabricated devices are in contrast with this picture and could represent the first evidence of short channel a-Si:H TFTs not limited by parasitic resistance. In fact, as shown in Fig.3 for devices where Al-contacts were used, the μ_{FE} values deduced for different L do not appreciably change, even in the submicron region. A temptative explanation for such behaviour could reside in the effects of Al-diffusion in the contact regions. In fact, Al is known[9,10] to diffuse at relatively low temperature in the a-Si:H. Such a diffusion can greatly affect the contact resistances as well as reduce the unaccumulated a-Si:H path. This last case, we believe, is the major cause of reduction of parasitic resistance in our devices, where rather thin n^+ a-Si:H and a-Si:H layers are employed (even a Al-diffusion of a few hundred angstroms can have a drastic effect). This effect, of course, can be much less evident for devices where relatively thick a-Si:H layers are employed and, in fact, no appreciable improvements in our conventional TFTs are observed after 200 °C annealing.

In Fig.5 the $I_d^{1/2}$ vs V_g is shown for different channel lengths and it can be recognized a rather large effective threshold voltage, $V_{th} \sim 11$ V, if compared to conventionally fabricated devices, $V_{th} \sim 1$ V [6]. This large V_{th} could result as an effect of the charging of localized deep states present in the gate insulator with back-scattered electrons, during the electron beam exposure.

It should be mentioned that preliminary data on Cr-contacts short-channel devices show a degradation of μ_{FE} with L, similarly to data reported in ref.5, where NiCr-contacts were used, confirming the role of Al-diffusion in obtainig low parasitic resistances. On the other hand, NiCr contacts[10] as well as Cr[9] contacts are reported not interact with a-Si:H at least for temperature up to 200 °C.

The output characteristics, I_d vs V_{ds}, at different V_g are reported in Fig.6 for three different channel lengths relative to devices where

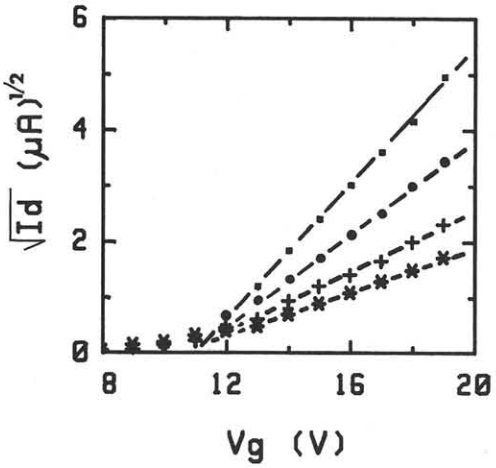

Fig.5 Saturated characteristics for Al-contacts TFTs, with W = 20 μm, at different channel length: (*) L = 9.5 μm, (+) L = 4.5 μm, (•) L = 1.7 μm, (▪) L = .7 μm.

Cr-contacts were used. In the long-channel case (10 μm) the I_d - V_{ds} curves show the typical saturation while in the case of submicron L short channel effects are clearly evident. The reduction, for increasing V_{ds}, of the effective channel length causes, in fact, a non-saturated I_d - V_{ds}, as for c-Si short-channel MOSFET[11].

4. CONCLUSIONS

Short-channel a-Si:H TFTs have been fabricated by direct writing EBL. In the case of Al source-drain contacts, no field-effect mobility degradation has been observed for submicron channel lengths, in contrast with already published data[5]. This result has been attributed to a drastic reduction of the parasitic resistance by the Al-diffusion in concomitance with the thin a-Si:H layer used. Thinner a-Si:H active layer could, in principle, till improve the characteristics of the devices, in terms of residual parasitic resistance as well as field-effect mobility[12], but a severe limitation in this sense comes from the control of the back-channel etching.

Modelling of short-channel devices is in progress in order to better understand the device physics of a-Si:H TFTs in the submicron regime.

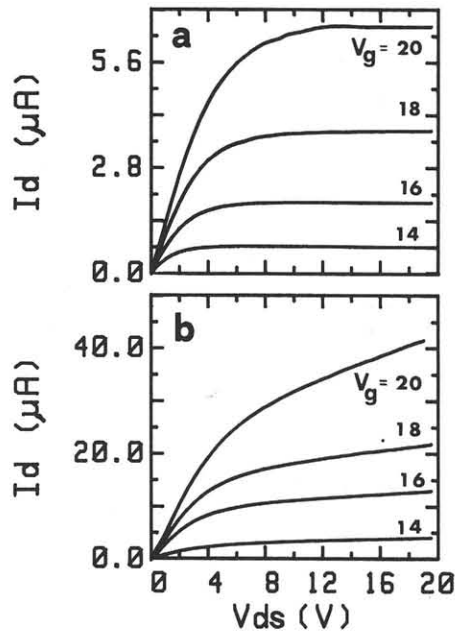

Fig.6 Output characteristics at different gate voltages for three different channel lengths, L, and W= 150 μm for EBL-devices with Cr source-drain contacts: a) L = 10 μm, b) L = .44 μm.

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