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Top-Gate Amorphous-Silicon Thin-Film Transistors Produced by CVD Method

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Chemical-vapor-deposited (CVD) amorphous-silicon films have been applied as the active layers in thin-film transistors with top-gate structure, for the first time. The maximum field-effect mobility and the typical on/off current-ratio were more than $0.5cm^2/Vs$ and 10^7, respectively. The characteristics were better than the ones based on plasma-CVD.

1. Introduction

Amorphous-silicon thin-film transistors (a-Si TFTs) have been extensively investigated for applying them into large-area flat-panel displays[1]. Displays with more than 10^6 pixels have been formed on a 14''-diagonal glass substrate. Although the present a-Si TFTs are formed by using plasma-CVD method[2] and have a bottom-gate structure[3], it becomes clear that the device structure and the processing technology should be improved for denser and larger displays with reasonable production cost.

We have investigated a new a-Si deposition method[4] by using a higher silane and demonstrated that good a-Si TFTs can be formed on glass substrate[5] by using a totally plasma-free (CVD) method.

This paper shows that the CVD method can also be applied to a top-gate structure which has the following advantages : Firstly, the top-gate TFTs can be produced by only 2 photomasks[6]. Secondly, the gate bus-line can be sufficiently thick, resulting in a small bus-line resistance. Thirdly, high mobility poly-silicon TFTs can be easily formed for peripheral circuits[7] together with a-Si TFTs in a matrix.

2. Formation of Thermally Stable Source and Drain Electrodes

A schematic cross sectional view is shown in Fig. 1 for the top-gate TFT under study. In order to form a good MIS interface, the source and drain electrodes should be formed before depositing the active a-Si layer. Since the CVD temperature of a-Si is more than 400°C, Al can not be used as source and drain electrodes due to degradation of TFT characteristics by alloying of a-Si with Al. It has been reported[8] that many metals make alloy with

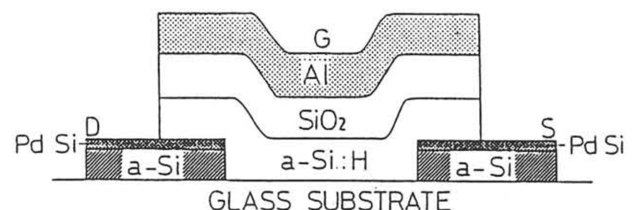

Fig.1 Schematic cross sectional view of the top-gate TFT under study.

single-crystal silicon at less than several hundred °C and that a-Si is chemically more active than single-crystal silicon[9]. Thus, pure metals will not be sufficiently stable for the source and drain.

We have used silicon-rich silicide for the source and drain because there remain no active metal molecules in this silicide. Palladium silicide was selected among many kinds of silicides since it can be formed at low temperatures and it is thermally stable.

Table I
Process Flow of Palladium Silicide Eledtrode

Step	Conditions
(1) CVD of a-Si	Si_3H_8 : 54sccm (diluted to 4% in Ar) H_2 : 62.5sccm P : 100Torr, T : 450°C
(2) Pd Evaporation	T : 150°C
(3) N_2 Annealing	N_2 : 200sccm P : 760Torr, T : 450°C
(4) Pd Removing	
(5) N_2 Annealing	N_2 : 200sccm P : 760Torr, T : 410°C

Palladium silicide was formed by the process flow tabulated in Table I. A 50 nm thick a-Si layer was deposited by thermal CVD method using a Si_3H_8-H_2 gas mixture at 450°C. Next, a 20 nm thick Pd layer was evaporated by using an electron beam. After the silicide was formed by heating the samples up to 450°C in nitrogen ambient, the remaining Pd metal was removed by iodine. The Si-rich palladium silicide was, then, annealed again at 410°C in order to finish the chemical reaction completely. The sheet resistivity of the electrode was 0.1Ω/square.

Thermally stable properties of the palladium silicide electrodes have been checked by a simple bottom-gate CVD a-Si TFT with thermal SiO_2 as a gate insulator and highly doped single-crystal Si substrate as the gate. The device has been heated in hydrogen ambient to various temperatures for 30 min. Hydrogen will remove from the film at temperatures more than 250°C and this will degradate device characteristics. In order to eliminate the change in characteristics caused by this de-hydrogenation, the devices were annealed again in hydrogen ambient at lower temperatures. The temperature and time of this annealing were changed to the optimum conditions for the highest mobility. The field-effect mobility was evaluated under low drain voltage conditions.

The results are shown by the solid curve in Fig. 2. The mobility was normalized by the mobility value μ_0 before annealing.

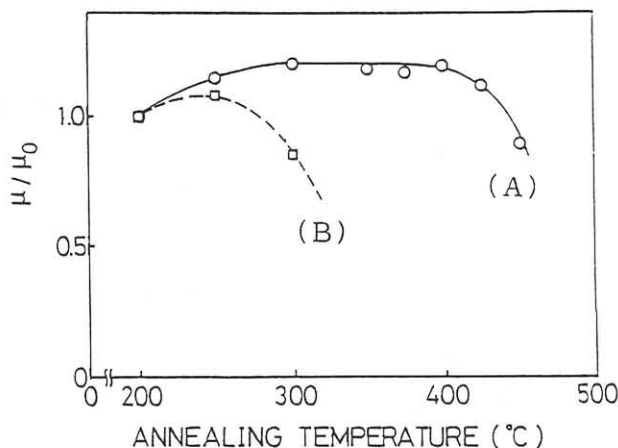

Fig.2 Field-effect mobility of the bottom-gate TFT as a function of the annealing temperature in hydrogen. The solid curve (A) is the palladium silicide TFT and the dashed curve (B) is the Aluminum TFT.

Characteristics of the bottom-gate TFT on the same chip but with Al electrodes on the CVD a-Si layer were also shown by the dashed curve for reference purpose. As can be seen the silicide TFT was not deteriorated in its

performance at least until 425°C, while the mobility of the Al TFT started to be decreased at temperatures as low as 250°C. Thus, it was concluded that silicide electrodes were thermally stable until the deposition temperature of thermal-CVD a-Si (400°C). It was observed that the surface of the silicide electrode was specular until 400°C, and began to be rough at more than 450°C.

3. Characteristics of The Top-Gate a-Si TFT

The top-gate TFT has been formed on a Corning 7059 glass substrate. After forming the silicide as the source and drain electrodes by the process flow listed in Table I, the a-Si and SiO_2 layers were deposited by the thermal CVD method using the process flow tabulated in Table II. The

Table II
Process Flow of TFT

Step	Conditions
(1) Palladium Silicide Forming & Patterning	
(2) CVD of a-Si	Si_3H_8 : 54sccm (diluted to 4% in Ar) H_2 : 62.5sccm P : 100Torr, T : 400°C
(3) H_2 Annealing	H_2 : 30sccm P : 76Torr, T : 250°C
(4) CVD of SiO_2	SiH_4 : 6sccm O_2 : 2sccm P : 0.8Torr, T : 250°C
(5) Al Evaporation & Patterning	
(6) H_2 Annealing	H_2 : 200sccm P : 760Torr, T : 250°C

a-Si layer was deposited at 400°C and was 50nm thick. In order to improve the CVD a-Si film, the samples were annealed at 250°C in hydrogen just before the deposition of SiO_2. For SiO_2 deposition, a gas mixture of silane (SiH_4) and oxygen was used. The deposition temperature was kept as low as the hydrogen annealing temperature (i.e., 250°C). The SiO_2 thickness was 140nm. An Al layer was evaporated on the SiO_2 layer as the gate electrode. After patterning the Al and SiO_2 layers, the samples were annealed again in hydrogen at 250°C. Channel length and width were 65μm and 220μm, respectively.

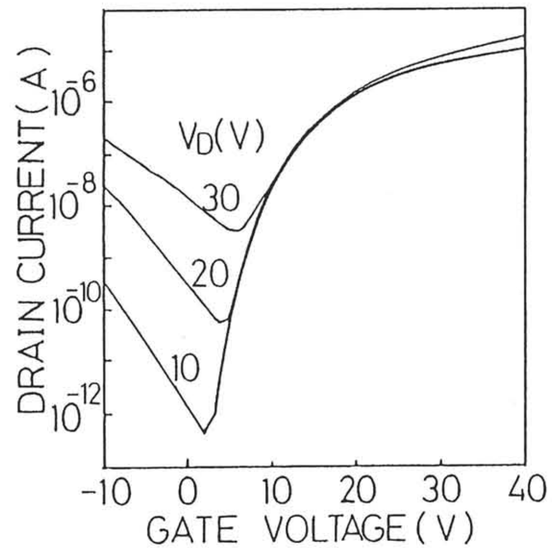

Fig.3 The semi-logarithmic drain current as a function of the gate voltage for various drain voltages.

The semi-logarithmic drain current, $\log(I_D)$, is shown in Fig. 3, as a function of the gate voltage V_G for drain voltages, V_D, of 10, 20 and 30V, respectively. The on/off ratio of the drain current was more than 10^7 at V_D=10V. The threshold voltage was 12.6V.

Linear I_D-V_D characteristics are shown in Fig. 4 for various positive V_G values. The maximum field-effect mobility estimated from the linear I_D-V_D region was 0.5 cm^2/Vs. These values are higher than typical values for the top-gate plasma-CVD TFT.[7)]

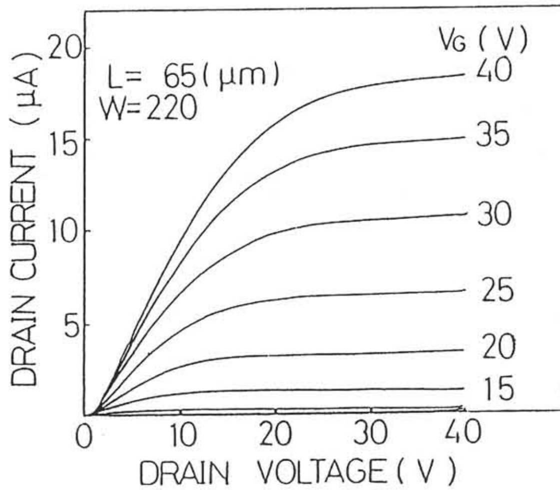

Fig.4 The drain current as a function of the drain voltage for various values of the gate voltage.

4. Conclusion

We have investigated an a-Si TFT with a top-gate structure. The high performance and simple fabrication steps of the CVD-produced top-gate TFT together with various advantages of CVD method[5] make this device very attractive for high quality displays.

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