Characteristics of a-Si TFTs Using Thermal-CVD-SiO₂/PECVD-SiNₓ Double Layered Gate Dielectrics

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We fabricated a-Si TFTs with thermal-CVD-grown-SiO₂/plasma-CVD-deposited-SiNx double layers as gate dielectrics, where a-Si:H was deposited on SiNx. Two kinds of films of APCVD or LPCVD grown SiO₂ were examined. TFT performance depends strongly on the growth temperature (Ts) of SiO₂. High performance TFTs, which have large field effect mobility of μ ~ 1 cm²/Vs and quite sufficient stability for practical application of TFT-LCDs, were obtained at Ts=430°C.

1. INTRODUCTION
SiNx) and SiOx) thin films deposited by plasma-enhanced chemical vapor deposition (PECVD) are widely used as gate dielectrics for amorphous silicon thin film transistors (a-Si TFT). A-Si TFTs using such films show threshold voltage instability caused by charge trapping in gate dielectrics. Thin films of SiO₂ grown by thermal-CVD are dense, contain neither N nor H, and have little carrier trapping states. Therefore, the improvement in TFT performance can be expected.

This paper presents characteristics of a-Si TFTs using Thermal-CVD-SiO₂/PECVD-SiNx double layered gate dielectrics, and compares them with that of TFTs using other gate dielectrics.

2. SAMPLE PREPARATION
a-Si TFTs with inverted staggered electrode structure were fabricated, as shown in Fig.1. Low resistivity molybdenum-tantalum (Mo-Ta) alloy was sputtered for a gate electrode. Thermal-CVD-SiO₂/PECVD-SiNx double layered structure was used for the gate dielectrics. Thin layers of PECVD-SiNx, 500A thick, and hydrogenated amorphous silicon (a-Si:H), 500A thick, were successively deposited in a single pump down to obtain a clean interface between them. SiNx acts as a Vth control layer to be around 2V. The 500A thick P-doped n+ microcrystalline silicon (n⁺μc-Si) layer was used for source and drain contacts. The 3500A thick SiO₂ films were grown by atmospheric (AP) CVD or low pressure (LP) CVD, using SiH₄, O₂ and N₂. In case of APCVD, the O₂/SiH₄ ratio was 20, while in case of LPCVD, the ratio was 2. The growth temperature (Ts) was varied between 350°C and 430°C.

3. SiO₂ FILM PROPERTIES
Figure 2 shows electron spin resonance (ESR) spectra for the SiO₂ film grown by
LPCVD at Ts=400°C and for SiOxNy films deposited by PECVD at Ts=330°C. The thickness of each film was 3500Å. SiOxNy films had large spin density caused by Si dangling bonds or O vacancies. Whereas, in case of SiOx, no signal attributed to spin was detected. Thus, LPCVD-SiO2 is a high quality material, whose spin density is less than 1 x 10^16 cm^-3.

Some properties for SiO2 films, grown by APCVD, are shown in Fig.3. Both refractive index and etching rate by buffered HF were independent from Ts, while O/Si ratio, measured with Rutherford backscattering spectroscopy, slightly increased with increasing Ts. It is considered that the film grown at 430°C has almost stoichiometric composition, and that films grown at low temperature are just a little silicon rich.

4. TFT CHARACTERISTICS

Figure 4 shows field effect mobility (μ) and threshold voltage (Vth) as a function of SiO2 growth temperature Ts values. Eight samples were measured at each Ts. When Ts=350°C, both μ and Vth scattered very much. However, it was observed that μ increased and Vth decreased with increasing Ts. When Ts=430°C, μ=1.0±0.2 cm^2/Vs and Vth=2.5±0.3V were obtained. These results suggest that TFT characteristics are mainly dominated by the SiNx/a-Si interface properties, and are also affected by the SiO2 bulk properties.

5. Vth INSTABILITY

Bias temperature stress (BTS) tests were examined. Figure 5 shows transfer characteristics for TFTs, before and after applying +15V (+BTS) or -15V (-BTS) to gate
electrodes at 80°C for 10000 seconds. SiO₂ films were grown by APCVD. In case (a), Ts=350°C, Vth shifts both by +BTS and by -BTS were extremely large. Additionally, a negative Vth shift was observed by +BTS. The authors considered that this strange behavior was attributed to hole injections from the gate electrode to SiO₂. In case (b), also where Ts=350°C, no negative shift by +BTS was observed. However, the Vth shift magnitude was still large. In both cases, Vth was unstable, even though initial TFT characteristics were nearly the same as Ts=430°C. In case (c), Ts=430°C, Vth shifts by +BTS and -BTS were only about 1V and -0.3V, respectively. It is considered that carrier trapping states in SiO₂ might decrease with increasing Ts.

Figure 6 shows Vth shift versus bias voltage curves for the TFTs using following gate dielectrics, APCVD-SiO₂(3500A)/SiNx(500A), LPCVD-SiO₂(3500A)/SiNx(500A), SiNx(4000A), PECVD-SiOₓNx(3500A)/SiNx(500A) and dip.coated-SiOₓ(3500A)/SiNx(500A). Although each TFT had the same SiNx/a-Si interface, there were many differences among their Vth shifts. PECVD-SiOₓNx/SiNx gate dielectric TFT showed +4V Vth shift by +15V BTS, while both APCVD and LPCVD showed +1V. Thus, TFTs using thermal-CVD-SiO₂/SiNx gate dielectric had much smaller shifts than the others.

Previously, it was reported that one of the Vth instability mechanism was charge trapping in SiNx, and that Vth instability depended strongly on SiNx/a-Si interface properties. Thus, it was thought that an improvement in its interface was the most effective way to decrease the Vth shift. However, the results presented in this paper suggest that the instability is dominated by the SiO₂ bulk properties, rather than SiNx/a-Si interface. Furthermore, the Vth...
shift decreases with decreasing total carrier trapping states in a gate dielectric. Thermal-CVD-SiO₂ films, both APCVD and LPCVD, are low defect materials. Therefore, very stable TFT can be obtained by using them.

6. TFT LIFETIME IN LCD OPERATION

Vth shifts for TFTs in liquid crystal display (LCD) operation were estimated by a computer simulation method, using the results of BTS tests. LCD addressing conditions for calculation are shown in Fig.7. The 25V value was used for gate voltage, but this condition was extremely unfavorable for the TFT stability. Figure 8 shows the calculated Vth shift versus LCD operating time curves for the TFTs using various gate dielectric structures. Environmental temperature was assumed to be 50°C. Assuming that an ultimate Vth shift value was 2V, the estimated lifetimes for TFTs, using PECVD-SiOₓ/SiNx or SiNx gate dielectrics, were below 10³ hours. In the case of a thermal-CVD-SiO₂/SiNx dielectric TFT, the lifetime reached 3x10⁴ hours.

7. CONCLUSION

The authors conclude that TFT performance is seriously affected by the bulk properties of gate dielectrics. Instability is especially dominated by the total carrier trapping states in gate dielectrics.

High performance TFTs, which have large field effect mobility, $\mu \sim 1$ cm²/vs, and quite sufficient stability for practical application of TFT-LCDs, are obtained by using thermal-CVD SiO₂ grown at Ts=430°C.

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REFERENCE