Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 1027-1030

S-E-23

Characteristics of a-Si TFTs Using Thermal-CVD-SiO_2/PECVD-SiN_x Double Layered Gate Dielectrics

KAICHI FUKUDA and NOBUKI IBARAKI

Electron Device Engineering Laboratory, Toshiba Corporation
8 Shinsugita-cho, Isogo-ku, Yokohama, Japan

We fabricated a-Si TFTs with thermal-CVD-grown-SiO_2/plasma-CVD-deposited-SiNx double layers as gate dielectrics, where a-Si:H was deposited on SiNx. Two kinds of films of APCVD or LPCVD grown SiO_2 were examined. TFT performance depends strongly on the growth temperature (Ts) of SiO_2. High performance TFTs, which have large field effect mobility of $\mu \sim 1 cm^2/vs$ and quite sufficient stability for practical application of TFT-LCDs, were obtained at Ts=430℃.

1. INTRODUCTION

SiNx[1] and SiOx[2] thin films deposited by plasma-enhanced chemical vapor deposition (PECVD) are widely used as gate dielectrics for amorphous silicon thin film transistors (a-Si TFT). A-Si TFTs using such films show threshold voltage instability caused by charge trapping in gate dielectrics.[3] Thin films of SiO_2 grown by thermal-CVD are dense, contain neither N nor H, and have little carrier trapping states. Therefore, the improvement in TFT performance can be expected.

This paper presents characteristics of a-Si TFTs using Thermal-CVD-SiO_2/PECVD-SiNx double layered gate dielectrics, and compares them with that of TFTs using other gate dielectrics.

2. SAMPLE PREPARATION

a-Si TFTs with inverted staggered electrode structure were fabricated, as shown in Fig.1. Low resistivity molybdenum-tantalum (Mo-Ta) alloy was sputtered for a gate electrode. Thermal-CVD-SiO_2/PECVD-SiNx double layered structure was used for the gate dielectrics. Thin layers of PECVD-SiNx, 500A thick, and hydrogenated amorphous silicon (a-Si:H), 500A thick, were successively deposited in a single pump down to obtain a clean interface between them. SiNx acts as a Vth control layer to be around 2V. The 500A thick P-doped n+ microcrystalline silicon ($n^+\mu$c-Si) layer was used for source and drain contacts. The 3500A thick SiO_2 films were grown by atmospheric (AP) CVD or low pressure (LP) CVD, using SiH_4, O_2 and N_2. In case of APCVD, the O_2/SiH_4 ratio was 20, while in case of LPCVD, the ratio was 2. The growth temperature (Ts) was varied between 350℃ and 430℃.

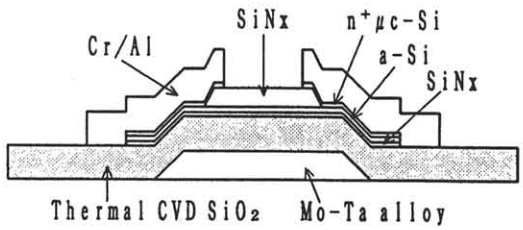

Fig.1 Schematic diagram of a-Si TFT.

3. SiO_2 FILM PROPERTIES

Figure 2 shows electron spin resonance (ESR) spectra for the SiO_2 film grown by

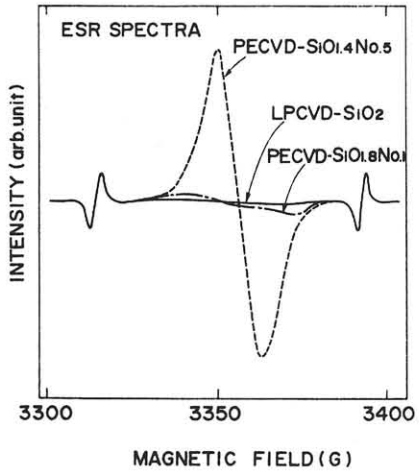

Fig.2 ESR spectra for SiOx films.

LPCVD at Ts=400℃ and for SiOxNy films deposited by PECVD at Ts=330℃. The thickness of each film was 3500A. SiOxNy films had large spin density caused by Si dangling bonds or O vacancies. Whereas, in case of SiO_2, no signal attributed to spin was detected. Thus, LPCVD-SiO_2 is a high quality material, whose spin density is less than 1×10^{16} cm^{-3}.

Some properties for SiO_2 films, grown by APCVD, are shown in Fig.3. Both refractive index and etching rate by buffered HF were independent from Ts, while, O/Si ratio, measured with Rutherford backscattering spectroscopy, slightly increased with increasing Ts. It is considered that the film grown at 430℃ has almost stoichiometric composition, and that films grown at low temperature are just a little silicon rich.

4. TFT CHARACTERISTICS

Figure 4 shows field effect mobility (μ) and threshold voltage (Vth) as a function of SiO_2 growth temperature Ts values. Eight samples were measured at each Ts. When Ts=350℃, both μ and Vth scattered very much. However, it was observed that μ increased and Vth decreased with increasing Ts. When Ts=430℃, $\mu = 1.0 \pm 0.2 cm^2/vs$ and Vth=2.5±0.3V were obtained. These results

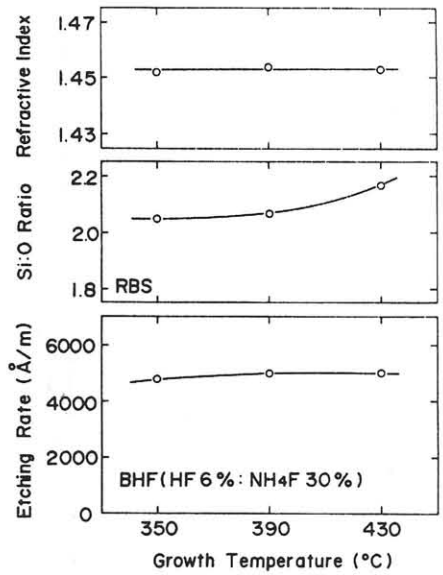

Fig.3 SiO_2 film properties for several growth temperature.

suggest that TFT characteristics are mainly dominated by the SiNx/a-Si interface properties, and are also affected by the SiO_2 bulk properties.

5. Vth INSTABILITY

Bias temperature stress (BTS) tests were examined.[4] Figure 5 shows transfer characteristics for TFTs, before and after applying +15V (+BTS) or -15V (-BTS) to gate

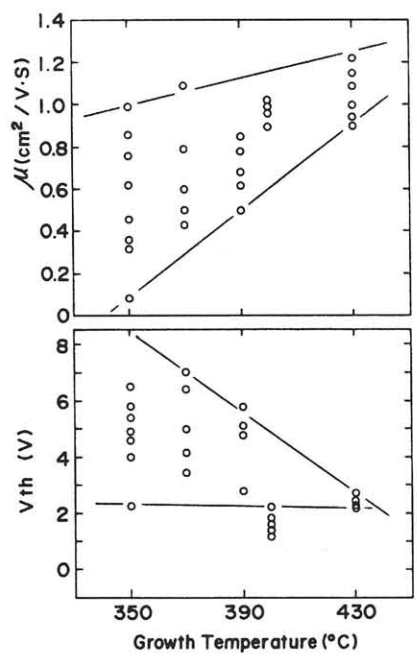

Fig.4 TFT characteristics, μ and Vth, as a function of Ts.

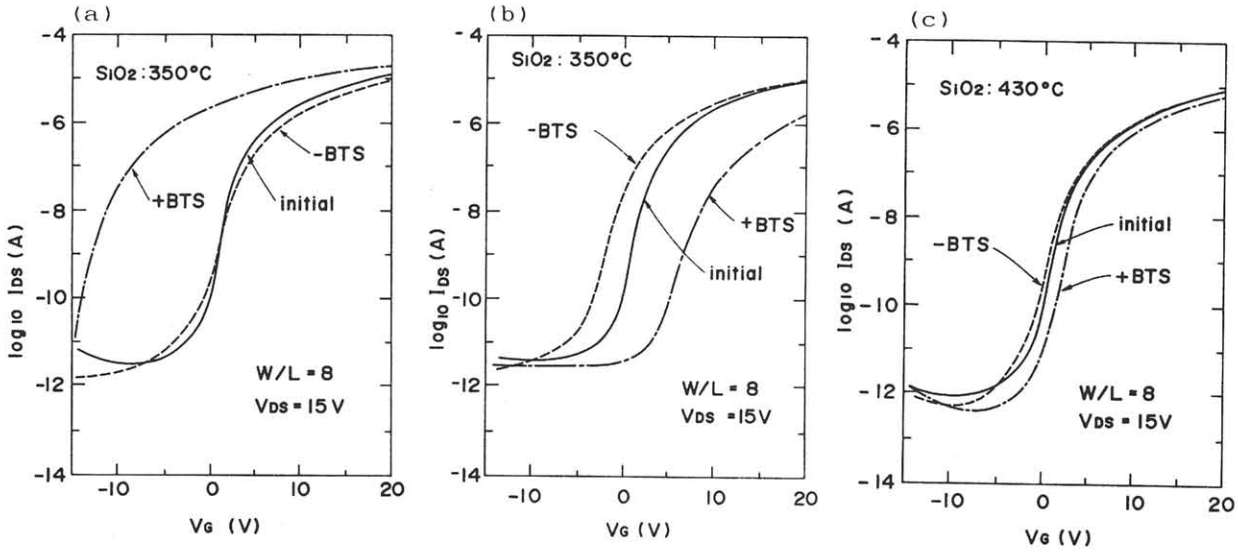

Fig.5 Transfer characteristics, before and after applying bias temperature stress.

electrodes at 80℃ for 10000 seconds. SiO_2 films were grown by APCVD. In case (a), Ts=350℃, Vth shifts both by +BTS and by -BTS were extremely large. Additionally, a negative Vth shift was observed by +BTS. The authors considered that this strange behavior was attributed to hole injections from the gate electrode to SiO_2. In case (b), also where Ts=350℃, no negative shift by +BTS was observed. However, the Vth shift magnitude was still large. In both cases, Vth was unstable, even though initial TFT characteristics were nearly the same as Ts=430℃. In case (c), Ts=430℃, Vth shifts by +BTS and -BTS were only about 1V and -0.3V, respectively. It is considered that carrier trapping states in SiO_2 might decrease with increasing Ts.

Figure 6 shows Vth shift versus bias voltage curves for the TFTs using following gate dielectrics, APCVD-SiO_2(3500A)/SiNx(500A), LPCVD-SiO_2(3500A)/SiNx(500A), SiNx(4000A), PECVD-SiOxNy(3500A)/SiNx(500A) and dip.coated-SiOx(3500A)/SiNx(500A). Although each TFT had the same SiNx/a-Si interface, there were many differences among their Vth shifts. PECVD-SiOxNy/SiNx gate dielectric TFT showed +4V Vth shift by +15V BTS, while,both APCVD and LPCVD showed +1V. Thus, TFTs using thermal-CVD-SiO_2/SiNx gate dielectric had much smaller shifts than the others.

Previously, it was reported that one of the Vth instability mechanism was charge trapping in SiNx[5], and that Vth instability depended strongly on SiNx/a-Si interface properties.[6] Thus, it was thought that an improvement in its interface was the most effective way to decrease the Vth shift.[6][7] However, the results presented in this paper suggest that the instability is dominated by the SiO_2 bulk properties, rather than SiNx/a-Si interface. Furthermore, the Vth

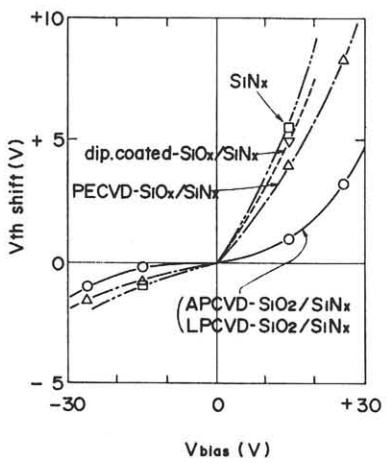

Fig.6 Vth shift vs. bias voltage curves for the TFTs using various gate dielectric structures.

shift decreases with decreasing total carrier trapping states in a gate dielectric. Thermal-CVD-SiO_2 films, both APCVD and LPCVD, are low defect materials. Therefore, very stable TFT can be obtained by using them.

6. TFT LIFETIME IN LCD OPERATION

Vth shifts for TFTs in liquid crystal display (LCD) operation were estimated by a computer simulation method, using the results of BTS tests.[4] LCD addressing conditions for calculation are shown in Fig.7. The 26V value was used for gate voltage, but this condition was extremely unfavorable for the TFT stability. Figure 8 shows the calculated Vth shift versus LCD operating time curves for the TFTs using various gate dielectric structures. Environmental temperature was assumed to be 50℃. Assuming that an ultimate Vth shift value was 2V, the estimated lifetimes for TFTs, using PECVD-SiOx/SiNx or SiNx gate dielectrics, were below 10^3 hours. In the case of a thermal-CVD-SiO_2/SiNx dielectric TFT, the lifetime reached 3×10^4 hours.

7. CONCLUSION

The authors conclude that TFT performance is seriously affected by the bulk properties of gate dielectrics. Instability is especially dominated by the total carrier trapping states in gate dielectrics.

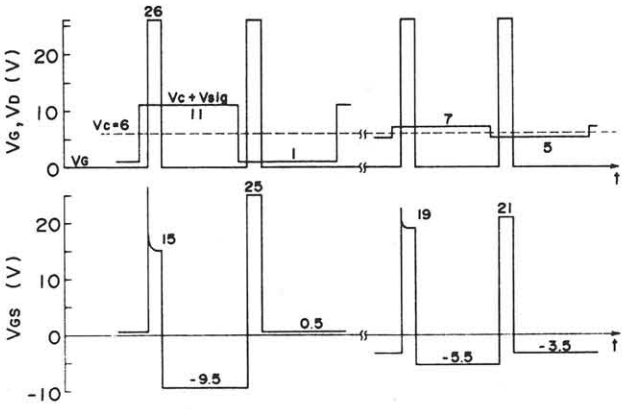

Fig.7 LCD addressing conditions used for lifetime calculation.

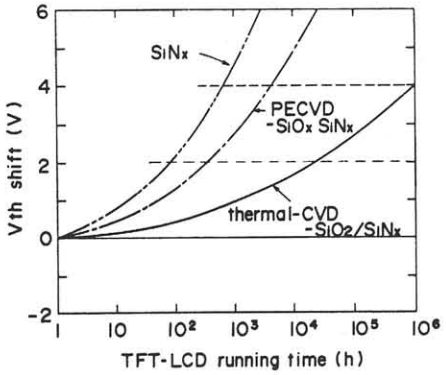

Fig.8 Calculated Vth shift vs. LCD operating time curves for the TFTs using various gate dielectric structures.

High performance TFTs, which have large field effect mobility, $\mu \sim 1$ cm^2/vs, and quite sufficient stability for practical application of TFT-LCDs, are obtained by using thermal-CVD SiO_2 grown at Ts=430℃.

ACKNOWLEDGMENTS

The authors wish to thank H.Ito, N.Hirata, K.Matsumura and T.Takehara for their useful discussions and experimental assistance.

REFERENCE

1. P.G.LeComber, W.E.Spear and A.Ghaith, Electron.Lett.15 (1979) 179
2. M.Ikeda, M.Dohjo and T.Aoki, Jpn.J.Appl. Phys.1,26 (1987) 1563
3. M.J.Powell, Appl.Phys.Lett.43 (1983) 597
4. N.Ibaraki, M.Kigoshi, K.Fukuda, and J. Kobayashi, J.Non-Cryst.Solids 115 (1989) 138
5. M.J.Powell, C.van Berkel, I.D.French, and D. H.Nicholls, Appl.Phys.Lett.51 (1987) 1242
6. Y.Kaneko, A.Sasano, T.Tsukada, R.Oritsuki and K.Suzuki, Extended Abstracts of the 18th Int.Conf.on Solid State Devices and Materials (1986) 699
7. N.Lustig, and J.Kanicki, J.Appl.Phys.65 (1989) 3951