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Correlation between Density of States Distributions and the Fermi Level Position in Interfacial Regions of Amorphous Silicon Thin Film Transistors

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This paper investigates the variation of the integrated density of states with conduction activation energy in hydrogenated amorphous silicon thin film transistors. Results are given for two different gate insulator layers, PECVD silicon oxide and thermally grown silicon dioxide. The different gate insulators produce transistors with very different initial transfer characteristics, but the variation of integrated density of states with conduction activation energy is shown to be similar.

The defect pool concept has recently been proposed by Smith and Wagner[1]. The central feature of this model is that there is a pool of potential defects which have a spread in formation energies, due to variations in local bonding environments. At elevated temperatures an equilibrium exists between defects, potential defect sites, and charge carriers. If the carrier concentration is changed, ie the Fermi energy is moved, then the equilibrium of defects with a particular formation energy is changed. Only those defects with a low formation energy are formed, while those with a high formation energy are potential defect sites. Thus as the Fermi level is raised towards the conduction band, defects will tend to form low in the energy gap, near to the valence band. Conversely if the Fermi level is lowered towards the valence band, then defects will tend to form high in the energy gap, near to the conduction band. As the sample is cooled the equilibrium is frozen into the lattice and the density of states becomes fixed. At room temperature extra defect states can be created, eg by light soaking or bias stress, but annealing rates are insignificant.

Bias annealing can be used to investigate these phenomena in amorphous silicon thin film transistors (TFTs)[2,3]. In this technique a gate bias is applied to the TFT during an annealing cycle. The annealing cycle used is a temperature ramp up to 180°C and down to 40°C at 0.1 °C/s. This causes the interfacial region of the TFT to equilibrate with the Fermi energy displaced from its position with no applied bias. The field effect density of states can be computed from the transistor transfer characteristics[4]. The total amount of charge needed to move from the electron to the hole conduction threshold is easily measured. Assuming the states swept are amphoteric dangling bonds this charge is numerically equal to twice the number of bonds the Fermi level is swept through.

We have conducted these experiments on transistors fabricated with a thermally grown oxide gate insulator, or a deposited silicon oxide gate insulator. The deposited oxide was grown by PECVD of SiH_4 and N_2O to a thickness of 0.5μm[5]. The thermal oxide was 0.2μm, grown on a heavily n-type doped silicon wafer. Interfaces of amorphous silicon with thermal oxide are in electron depletion with activation energy of conduction 1eV, whilst the interface with our PECVD oxide is in electron accumulation due to a positive fixed charge, with activation energy of conduction 0.57eV.

The measured threshold voltages, changes of threshold voltage and conduction activation energies for various bias anneals are presented in tables 1 and 2.

As can be seen the deposited oxide threshold voltage shifts are far form symmetrical. We attribute this to charge trapping in the gate insulator, observed also in room temperature bias stressing measurements. In figure 1 we plot the capacitance of the insulator multiplied by the total voltage between electron and hole thresholds. In figure 2 these results are plotted relative to the minimum for each sample.

The variation of the integrated density of states with Fermi level position, shown in figure 2, shows a similar dependence for the thermal and deposited oxide samples. Note that the TFTs when first produced were at different points on this curve, due to different fixed charges in the gate insulator layer. The PECVD oxide has a positive fixed charge, like PECVD silicon nitride insulators. This results in the TFT interface being in electron accumulation, so when the devices are annealed the density of states equilibrates to have the majority of defects near the valence band, and few near the conduction band. This results in a steep prethreshold slope for electron conduction and a shallow prethreshold slope for hole conduction. In the thermal oxide the interface is in electron depletion, resulting in the majority of states being near the conduction band. Thus it has a shallower prethreshold slope for electron conduction, and a steeper prethreshold slope for hole conduction. As was shown in a previous paper[2], as the thermal oxide is bias annealed with positive gate biases the density of states changes to become similar to a PECVD silicon nitride TFT density of states[6] shown in figures 3. As the Fermi level moves from about 1eV to 0.8eV below the conduction band edge the total number of states is roughly constant, but the energy distribution changes dramatically[2,3]. The PECVD oxide has a slightly lower minimum total number of states than the thermal oxide. These samples were made in different reactors, so this could result from differences in the amorphous silicon layer, perhaps from differing sizes of the defect pool due to differing levels of disorder in the lattice, different hydrogen incorporation, or different levels of mechanical stress occurring at the interface.

In conclusion it is clear form figures 1-3 that the Fermi level position determines the density of states distribution and total number of states at the interfacial region of amorphous silicon TFTs. If the Fermi level is moved nearer to the valence band more defects are created in the upper part of the energy gap. If the Fermi level is moved nearer to the conduction band then more defects are created in the lower part of the energy gap. This paper has shown that this is independent of the gate insulator. The main effect of the gate insulator being how its associated fixed charge affects the Fermi level position at the interface.

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Table 1: Threshold Variation With Bias Annealing For Thermal Oxide.

Anneal Voltage (V)	V_{te} (V)	V_{th} (V)	E_a (eV)
-10	25.0	-17.7	0.80
-5	21.0	-12.9	0.88
0	16.0	-10.0	1.00
5	16.0	-10.8	0.84
10	17.0	-11.0	0.75
15	20.2	-14.0	0.65
20	24.2	-16.1	0.60
25	28.5	-19.5	0.56

Table 2: Threshold Variation With Bias Annealing For PECVD Oxide.

Anneal Voltage (V)	V_{te} (V)	V_{th} (V)	E_a (eV)
-70	-38.7	-93.0	0.968
-60	-31.8	-85.5	0.861
-50	-25.3	-77.7	0.844
-40	-18.2	-73.0	0.831
-30	-11.6	-67.4	0.797
-20	-2.7	-65.1	0.721
0	9.3	-70.0	0.500

Figure 1: Variation Of $C(V_{te}-V_{th})/q$ With Bias Annealing

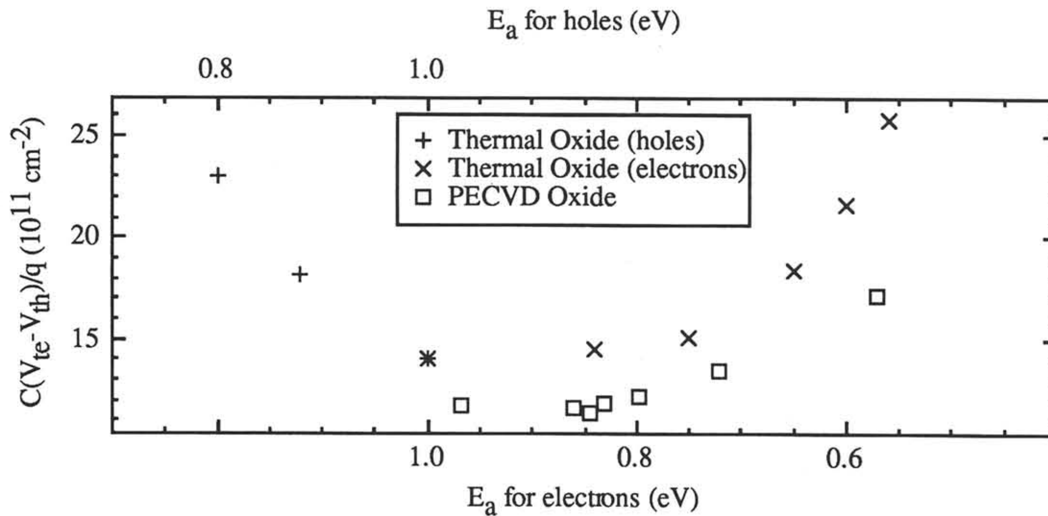

Figure 2: Variation Of $C(dV_{te}+dV_{th})/q$ With Bias Annealing

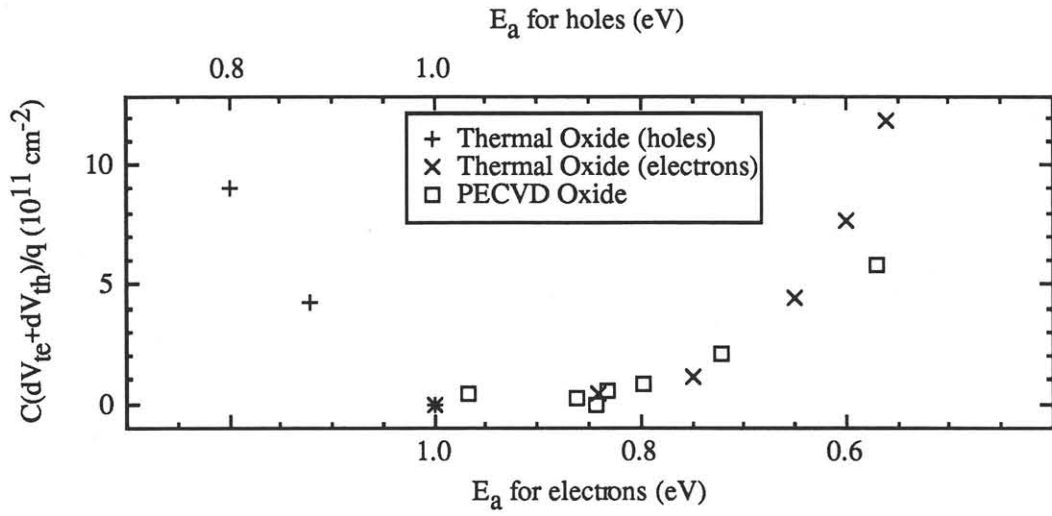

Figure 3: DOS For Bias Annealed Thermal Oxide