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Mechanism of Mobility Improvement of a-Si TFT with Channel Passivated Layer

Yasuo TANAKA, Ken TSUTSUI, Toshiko KOIZUMI†,
Hideaki YAMAMOTO and Toshihisa TSUKADA

Central Research Laboratory, Hitachi, Ltd.,
† Musashino Works, Hitachi Device, Ltd.,
Kokubunji, Tokyo 185, Japan

The a-Si TFT with the channel-passivated layer shows high mobility and low threshold-voltage compared with the conventional TFT. The βmax^{-1} vs. channel-length relations indicate the existence of the induced n-channel under the drain/channel-passivation overlap region for Vg<Vd. The induced-channel shortens the effective channel-length to increase the observed mobility, and that suppresses the hole-injection from drain-electrode in Vg<0V. Optimizing the conditions of depositing a-Si(i) layer, the off-current at Vg=-20V decreases lower than 10^{-13}A.

1. Introduction

The a-Si TFT's have been widely used in active-matrix liquid crystal displays (LCD's) [1]. The requirements of a-Si TFT's for TFT/LCD's are high on-current for signal-charging, low off-current(Ioff) for signal- holding [2], low threshold-voltage(Vt) for reducing driving voltage and small Vt-shift for reliability [3]. Several types of structures have been proposed on the a-Si TFT's, so far. The inverted-gate-staggered a-Si TFT with the channel-passivated (CHP) layer has advantages of high mobility [4] and low off-current. However, it is not always clear why the CHP-TFT has these merits. Recently, the overlap-effects of CHP-TFT's were calculated using two-dimensional computer simulations [5]. We studied experimentally some ambiguous points to estimate the mobility (μ), the Vt and the Ioff in the CHP-TFT's. Such conditions as the applied-voltages on the gate (Vg) and drain electrodes (Vd), the sizes of channel-width (W) and length (L) after fabrication, and the edge-effects should be taken into account carefully. In this paper, we will discuss the mechanism of the mobility increase and the Vt reduction, and the conditions to lower off-currents in the CHP-TFT's.

2. Experiment

2.1 TFT Fabrication

Fig. 1 shows the cross-sectional view of an asymmetrical CHP-TFT in which the overlap-lengths of source/CHP and drain/CHP are made asymmetrically. On a glass substrate, a gate-electrode of Cr was formed, on which a gate-insulator of SiN(300 nm thickness), an undoped a-Si(i) layer(20 ~ 50 nm) and a CHP layer of SiN(200 nm) is continuously deposited by the rf(13.56 MHz) glow-discharge CVD method. The SiH_4-NH_3-N_2 mixtures were used for the depositions of the gate-insulator and the CHP layer, the pure SiH_4 was used for the a-Si(i) layer. The a-Si(i) layer degradation were prevented by controling deposition temperature of the a-Si(i) and CHP layer. After the CHP patterns were formed, a light etch was necessary over the a-Si(i) surface by a diluted HF-NH_4F buffer-solution to improve the source and drain contacts. Then, an a-Si(n^+) layer(30 nm) was deposited by the same CVD method using the SiH_4-H_2-PH_3 mixtures. The a-Si(n^+) layer

on the CHP layer was removed after the formation of source-drain electrodes of evaporated Cr and Al. Finally, a passivation layer was formed (not shown in Fig. 1).

2.2 Measurement

First, the overlap-effects of drain-electrode over the CHP layer on the CHP-TFT is investigated by comparison with the conventional inverted-gate-staggered TFT in which an a-Si(n^+) layer is deposited continuously on an a-Si(i) layer. We define the channel-length under the CHP layer as L, and the drain/CHP overlap-length as ΔOL. The μ and β values are derived from the differential curves of the $\sqrt{Id}$ vs. Vg curves using the relation of $\sqrt{Id} = \sqrt{(\beta/2)}\cdot(Vg-Vt)$, where $\beta = \mu\cdot C_{SiN}\cdot W/L$, Id is the drain-current, and C_{SiN} is the capacitance of the SiN gate-insulator per unit area. In those curves, we define the maximum values of β and μ as βmax and μmax, respectively. The Vt,max and Vg,max correspond to those maximum values using the relations of $\sqrt{Id} = \sqrt{(\beta max/2)}\cdot(Vg,max-Vt,max)$ and $\beta max = \mu max\cdot C_{SiN}\cdot W/L$.

3. Results and Discussion

3.1 Dependences of μ and Vt on gate-voltage

Fig. 2 shows the μ vs. Vg and Vt vs. Vg characteristics for the CHP-TFT (L = 10.1 μm, ○ plots) and for the conventional TFT (L = 11.5 μm, △ plots). Fig. 2 indicates that the mobility of the CHP-TFT has the large dependence on the gate-voltage, and has the maximum values (μmax = 0.92 $cm^2/V\cdot s$, Vt,max =1.2 V) at around Vg = 5V (Vg,max). The μ-values at a gate-voltage higher than 10V are similar to those of the conventional TFT. On the contrary, the conventional TFT has a moderate peak in mobility at around 10V (μmax = 0.54 $cm^2/V\cdot s$, Vt,max = 2.6 V). The CHP-TFT's have higher μmax-values and lower Vt,max-values than those of the conventional TFT's in the range of Vg < Vd.

3.2 Effects of the drain/CHP overlap region

Fig. 3 shows the βmax^{-1} vs. L characteristics of the asymmetrical CHP-TFT in which ΔOL is large (ΔOL = 4.8 μm, ○ plots), compared with those of the same TFT with the source and drain electrodes exchanged, i.e., ΔOL is small (ΔOL = 0.0 μm, □ plots). It is clear that the plots corresponding to the large ΔOL (○ plots) and the small ΔOL (□ plots) are on the separate lines. On the other hand, as for the symmetrical CHP-TFT shown in Fig. 4, these phenomena have not been observed, and the both lines are exactly matched each other. In Fig. 4, ΔOL is almost the same, i.e., one side is ΔOL = 1.7 μm, ○ plots, another side is ΔOL = 1.5 μm, □ plots. If we use the channel-length L' which is equal to L-ΔOL instead of the channel-length L shown in Fig. 1, then the line of the ΔOL = 4.8 μm (○ plots) shifts to the left, and the line after the correction (● plots) is the same as the line corresponding to the ΔOL = 0.0 μm (□ plots). This fact suggests that the existence of the induced n-channel under the ΔOL region shown in Fig. 1, and this dominates the drain-current characteristics in the low gate-voltage of Vg < Vd. Then the channel length L becomes shorter by ΔOL, and as a result, the observed mobility increases.

After the correction of the ΔOL-effect (● plots) in Fig. 2, the μmax-value of the CHP-TFT takes a lower value (μmax = 0.73 $cm^2/V\cdot s$) than the original value (0.92 $cm^2/V\cdot s$), but this value is still higher than that of the conventional TFT (0.54 $cm^2/V\cdot s$). That was mainly caused by the differences of the edge-effects of the drain-electrode in the CHP-TFT and the plasma-damages on a-Si(i) back-surface in the conventional TFT.

Fig. 5 (a) and (b) show the comparison of the μ vs. Vg characteristics of different ΔOL, i.e., (a) ΔOL = 1.4 μm and (b) ΔOL = 0.3 μm for different Vd. Fig. 5 (a) shows the typical μ vs. Vg curves of the CHP-TFT, while Fig. 5

(b) shows similar to those of the conventional TFT. The induced n-channel under the ΔOL region has the effect of accelerating the rise of on-current as well as shortening channel-length, and going with this, the Vt,max-values become lower as shown in Fig. 2 and Fig. 5.

3.3 Off-current of the CHP-TFT's

Discussing the off-current of a-Si TFT, we should distinguish the two types of off-currents. One has the dependence on Vg due to the rising of the hole-current, another has not the dependence on Vg due to simple leakage currents such as the surface or boundary leakage current. In the conventional TFT's, it is difficult to achieve the off-currents lower than 10^{-13} A at Vg = -20 V and Vd = 10 V, although it is easier to achieve at Vg = -5 V. Because, the conventional TFT's have a strong electric field around the edge of drain electrode and the hole-injection easily occur. However, the CHP-TFT's have a weak electric field under the drain-electrode due to the electrical shield-effect of the ΔOL region. Moreover, the induced n-channel of the ΔOL region blocks the hole-injection from drain-electrode under negative gate bias. Consequently, the hole-injection in the CHP-TFT's will be suppressed lower level than the conventional TFT. Fig. 6 shows the dependence of the Ioff-values at Vg = -20 V on deposition temperature of a-Si(i) layer. As was expected, the Ioff-value is kept lower than 10^{-13} A in the range lower than 230℃. However, in the range higher than 240℃, the Ioff-value increases exponentially with the deposition temperature of a-Si(i) layer. This fact is explained as follows: the increase of acceptor levels in a-Si(i) layer due to the hydrogen release from this layer makes easy the hole-injection from the a-Si(n^+)layer under drain-electrode. In Fig. 6,the influence of channel-length on off-current is relatively small. Thus, the off-currents of CHP-TFT's are lowered with the optimized a-Si(i) layer.

This condition is also useful to prevent the abnormal positive Vt-shift accompanied with moderating of the rise of on-current under the negative-stress.

4. Summary

The a-Si TFT with the channel-passivated layer show high mobility and low threshold-voltage compared with the conventional TFT's. The on-current for the CHP-TFT's has the dependence on the drain/CHP overlap-length ΔOL, and indicate the existence of the induced n-channel under the ΔOL region in the low gate-voltage of Vg < Vd. The induced n-channel shortens the effective channel length to increase the observed mobility, and accelerates the rise of mobility in the low gate-voltage region. Another effect of the induced n-channel is suppressing hole-injection from the drain electrode under negative gate-voltage. The off-currents of the CHP-TFT's are reduced to a level lower than 10^{-13} A at Vg = -20 V with the optimized a-Si(i) layer.

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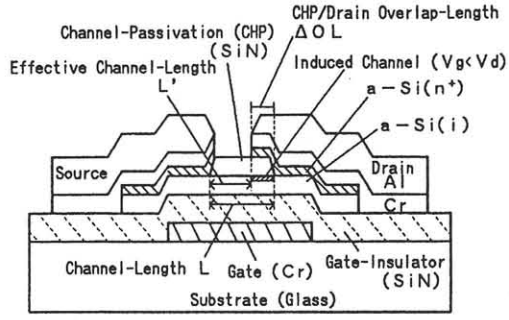

Fig. 1 Cross-sectional view of the asymmetrical CHP-TFT, with an overlap region of the drain-electrode on the channel-passivated layer.

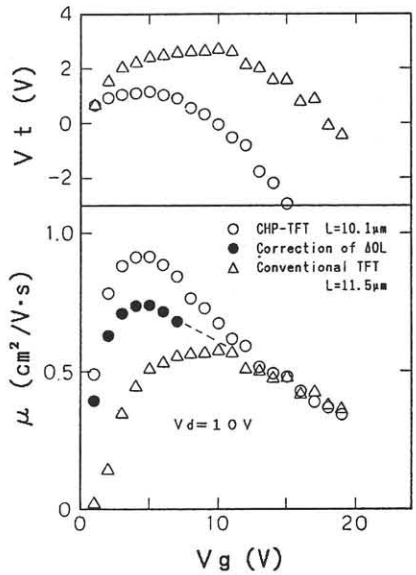

Fig. 2 μ and Vt vs. Vg characteristics of the symmetrical CHP-TFT (○) with the correction of ΔOL effect (●), compared with those of the conventional TFT (△).

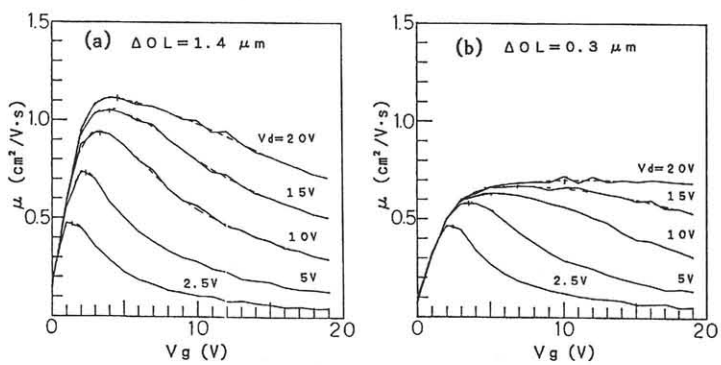

Fig. 5 Comparison of μ vs. Vg characteristics of different ΔOL, (a) ΔOL = 1.4 μm and (b) ΔOL = 0.3 μm for different Vd.

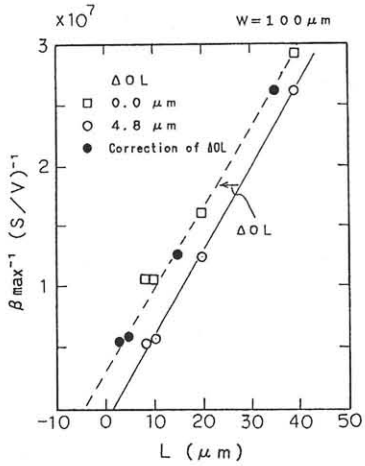

Fig. 3 βmax^{-1} vs. L characteristics of the asymmetrical CHP-TFT (ΔOL = 4.8 μm, ○) with the correction of the ΔOL effect (●), compared with those of the same TFT with the source and drain electrodes exchanged (ΔOL = 0.0 μm, □).

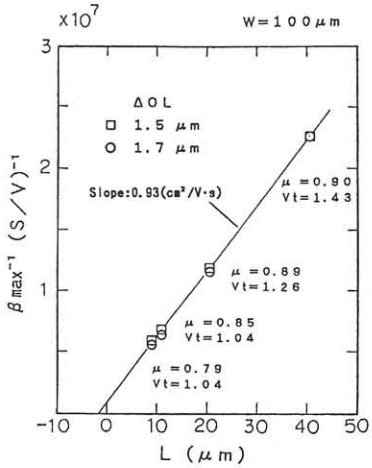

Fig. 4 βmax^{-1} vs. L characteristics of the symmetrical CHP-TFT (ΔOL = 1.7 μm, ○) compared with those of the same TFT with the source and drain electrodes exchanged (ΔOL = 1.5 μm, □).

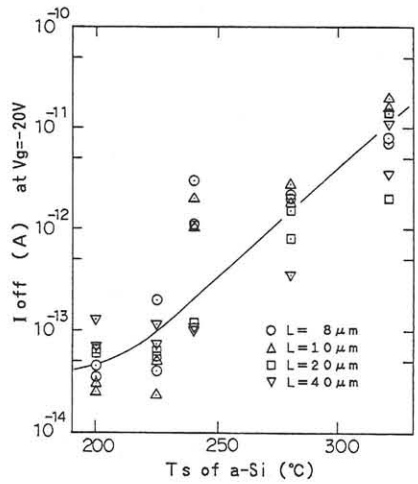

Fig. 6 Dependence of Ioff at Vg = -20 V on the deposition temperature of a-Si(i) layer.