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Invited

Large Area Amorphous Silicon vs Poly Silicon Devices

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The attributes and limitations of polysilicon and amorphous silicon devices are compared. The current process issues and device structures are summarized and the effects of stress are discussed. The state-of-the-art device and circuit performance are also described.

1. INTRODUCTION

Thin Film Transistors (TFTs) are the key devices in the large area electronic arrays used in active matrix liquid crystal displays, page width contact image sensors, and printers. This emerging technology will make a major impact on a wide range of products, generating a multi-billion dollar business. To meet the level of maturity of IC devices, many design, modeling, process, reliability and manufacturing issues need to be resolved. Amorphous silicon (a-Si) TFTs are more mature than polysilicon (p-Si) TFTs, but the latter offers considerable performance advantages, while not yet being manufacturable in large area. This paper reviews the present status of these devices.

The process temperature normally used in a-Si is 350°C, which enables the use of large area glass substrates like Corning 7059[1]. P-Si processes were first developed at 900-1000°C[2], thereby limiting the choice of substrate to quartz, which is very expensive. A low temperature (550-600°C) process has been developed so that the processes can be scaled to large area on glass substrates[2].

Comparing IC and large area (LA) electronics, the device operating voltages and device sizes are shown as a function of "chip" size in Fig. 1, for various applications. The excellent inter-device isolation inherent in TFT structures also offers advantages, for example, in simplifying high voltage device design and eliminating the latchup problem from CMOS circuits. Even though the device density is lower, the level of complexity of LA devices (i. e., number of devices per "chip") compares with that of VLSI chips.

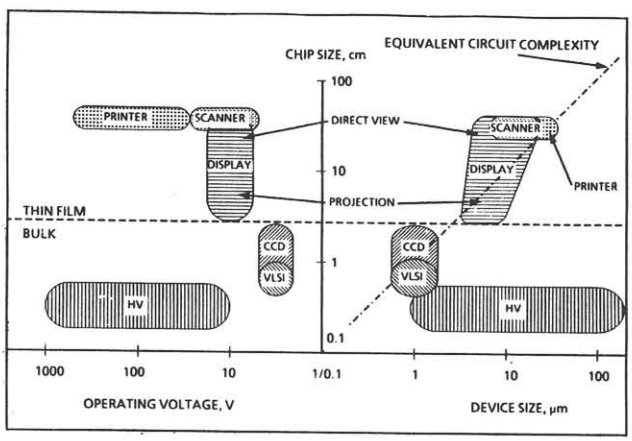

Fig. 1. Comparison of Thin Film & Bulk Si Devices

2. COMPARISON OF DEVICE CHARACTERISTICS

The current-voltage characteristics for a-Si and p-Si TFTs are shown in Fig. 2. The p-Si devices show useful n- and p-channel performance, whereas no significant p-channel operation has been observed in a-Si. The high temperature (HT) p-Si process includes two steps not used in the low temperature (LT < 600°C) process: a silicon self implant to enhance grain

size[3] and a high temperature anneal in an oxygen ambient to grow a thin layer of thermal oxide at the SiO_2/Si interface[4]. This enhancement of grain size results in a mobility of 100 cm^2/ Vs for the HT, compared with 40 cm^2/Vs for the LT device. The most pronounced difference between HT and LT technologies is the p-channel performance. The threshold voltage is 8.5 V and the mobility is 13 cm^2/ Vs for the LT TFT, compared with -2.6V and 50 cm^2/Vs for the HV TFT. This difference in device performance significantly affects the CMOS

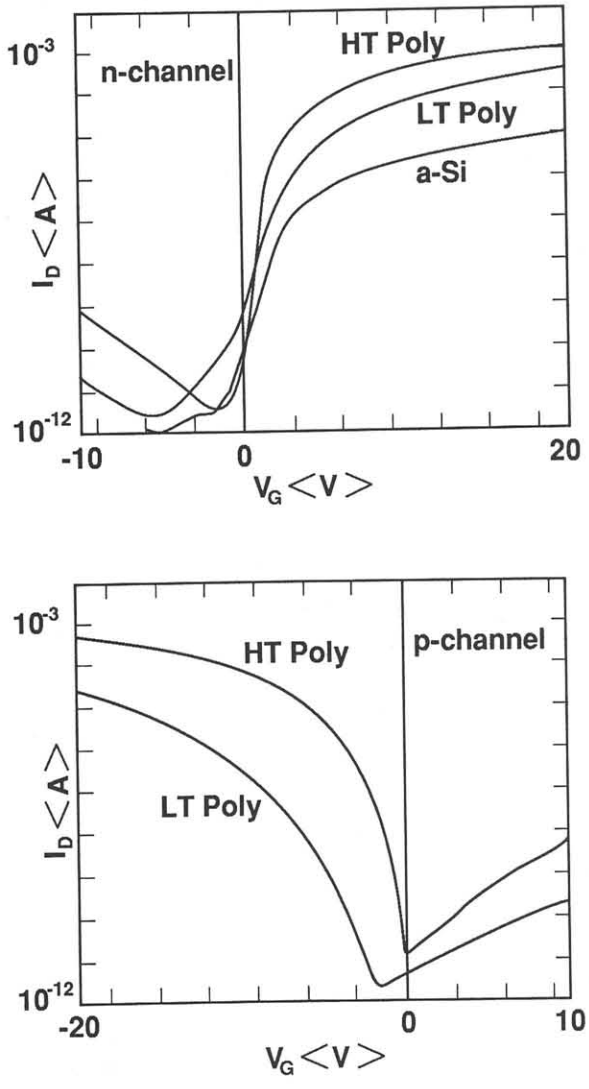

Fig. 2. Current-Voltage Characterictic of HT & LT p-Si and a-Si TFTs

operation for the LT process. The a-Si device has a mobility of 1 cm^2/Vs and, therefore, has considerable less drive current than the polysilicon TFTs; however, the off current is extremely low. Two dimensional numerical simulations have been successfully used to predict and analyze the behavior of both a-Si and p-Si TFTs (see Hack and Shaw, this proceedings).

3. a-Si PROCESS AND DEVICE STRUCTURE

Two relatively mature processes and device structures are commonly used. Both have a bottom gate as shown in Fig. 3. One uses a nitride-silicon-nitride structure incorporating a thin intrinsic layer (about 500Å), which enables self alignment and reduces the light sensitivity of the TFT (important in displays) but has more mask levels. The second is a nitride-silicon-n+silicon structure, which enables shorter channel length devices to be fabricated more easily but, as there is no selective etch between N^+ and intrinsic a-Si, a thick i-layer must be used. This will have high light sensitivity and prevent self alignment, which is accomplished by illuminating through the substrate intrinsic layer. Self aligned structures are important because they reduce voltage feedthrough in active matrix pixels by decreasing the gate drain capacitances. In addition, this eliminates a critical alignment step and increases yield and process latitude. However, light leakage can occur around the gate, which increases the off current and degrades the TFT performance in a display.

Many possible applications of TFTs require drive voltages well in excess of 100V; for example, ferroelectric liquid crystals, electrophoretic or PLZT electro-optic displays, and electrographic plotters. For these

applications, a high voltage TFT (HVTFT) is needed.

Fig. 3 shows a cross section of an HVTFT and it's I_DV_D characteristics. The device can be thought of as an accumulation mode MOSFET with an offset drain. The offset prevents an excess field from causing the silicon nitride gate insulator to break down. Because of its low conductivity, the intrinsic a-Si has low off current, although it is slightly n-type. The gated region controls the current flow in the same way as in the LVTFT; saturation occurs at higher drain voltages, due to the drop across the offset region length L_2. At drain voltages below saturation, the current flow in the offset region is space charge limited.

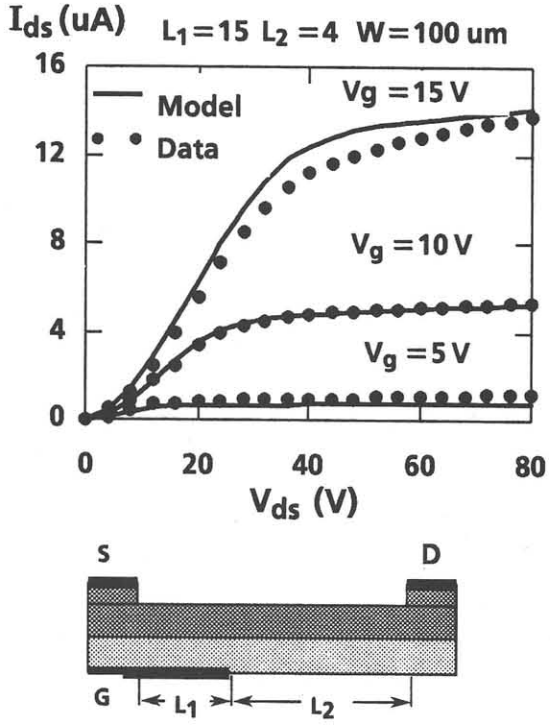

Fig. 3. Computed and experimental output data for a-Si high voltage TFT

The transistors have been modeled both analytically and by two dimensional numeric simulation. Fig. 3 shows the excellent fit of the numeric simulation[5].

If not designed properly, HVTFTs are susceptible to large shifts in their output characteristics. The drain voltage for a fixed drain current can translate to higher V_D when stressed with V_D high and V_G low. This shift to higher values is undesirable because it degrades the performance of the HVTFT in circuit applications. The shift depends only on the most recently applied voltages and saturates on the time scale of minutes. The shift arises from the creation of localized charge in the offset region near the gate edge. The charge comes from changes in the local density of states associated with the depletion of electrons below the intrinsic level caused by the off state drain stress.

Stability is insured by proper design of the HVTFT, in particular, the addition of a field plate.

4. AMORPHOUS SILICON DEVICE STABILITY

Under stress conditions the threshold voltage of a conventional a-Si TFT increases with time. This occurs because, in response to changes in the Fermi level position as the channel is accumulated with electrons, the a-Si attempts to restore the Fermi level back towards the midgap, the most stable thermodynamic state. Defects are created due to hydrogen diffusion in the material. The threshold shift will slowly recover with time without any applied bias. Hack, et al have recently shown that the recovery process is considerably speeded up when a lightly doped compensation layer is placed adjacent to the active layer in the transistor (see Fig. 4).

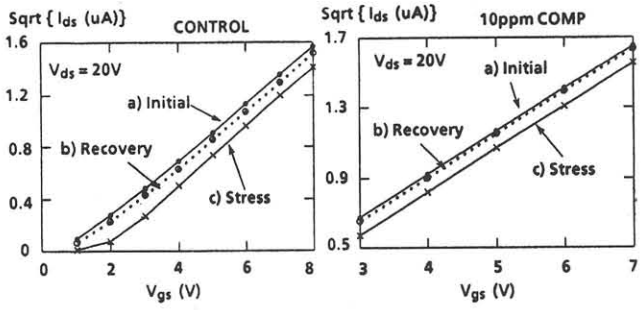

Fig. 4. (a) Transfer data for control and 10ppm proximity recovery a-Si TFT for a) initial state b) stressed state at room temperature for 20 minutes with $V_{gs} = V_{ds} = 20V$, and c) recovery at room temperature for 2 hours

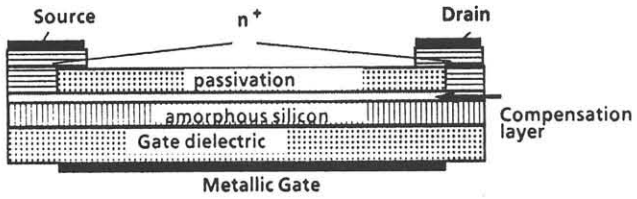

Fig. 4. (b) Conventional a-Si TFT with proximity recovery layer

5. POLYSILICON PROCESS AND DEVICE STRUCTURE

The device structure of a top gate ion implanted source/drain (S/D) TFT is shown in Fig. 5, alongside a deposited S/D bottom gate device. Neither of these processes is particularly mature, but large area print arrays have been produced using the former[6]. The choice of device structures and process architecture will be a tradeoff of device performance, process latitude, manufacturing throughput and scalability to large area. The deposited source/drain device has a lower mobility (~12 cm^2/Vs)[7], which may be due to a native film existing at the channel in the interface between the silicon layer and the source/drain film.

A critical step in the p-Si process is hydrogenation, which reduces the trap density and improves the TFT performance. The mobility is increased from 4.6 to 40 cm^2/Vs, in the LT process, the threshold voltage is shifted and the inverse subthreshold slope is reduced from 2.1 V/decade to 0.55 V/decade, following hydrogenation[8]. Significant process development is required to develop the optimum large area p-Si process. The focus is on obtaining large grain poly, a high quality gate dielectric ,and reducing annealing times.

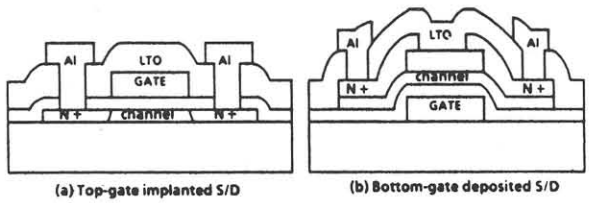

Fig. 5. The schematics of (a). top-gate, and (b) bottom-gate p-Si TFT cross-section

6. POLYSILICON DEVICE STABILITY

Polysilicon device degradation with electrical stress is relatively small compared with that of a-Si TFTs. The C-V data, upon electrical stress[4], suggests that interface states do not play a role in the degradation, which is predominantly due to metastable defect creation within the channel. This is similar to the mechanism observed in a -Si[9].

7. POLYSILICON SHORT CHANNEL EFFECTS

As performance and complexity requirements increase, there is a need to scale down device geometries to achieve higher speeds and packing densities. It has been shown that channel avalanche multiplication[10] is the dominant mechanism giving rise to short channel threshold shifts in p-Si TFTs at moderate or high drain bias. The effects are greater in NMOS TFTs than PMOS, due to the higher ionization rates for electrons in comparison to

holes. At low drain bias, a charge sharing mechanism dominates and the threshold shifts are small, at least in hydrogenated TFTs (see Fig. 6). Device design parameters, such as gate oxide or active island thickness, have little influence, and the most effective method for reducing the threshold shifts is to lower the supply voltage. When the supply voltage is lowered, device gate lengths can be reduced, but this does not necessarily improve circuit speed[10].

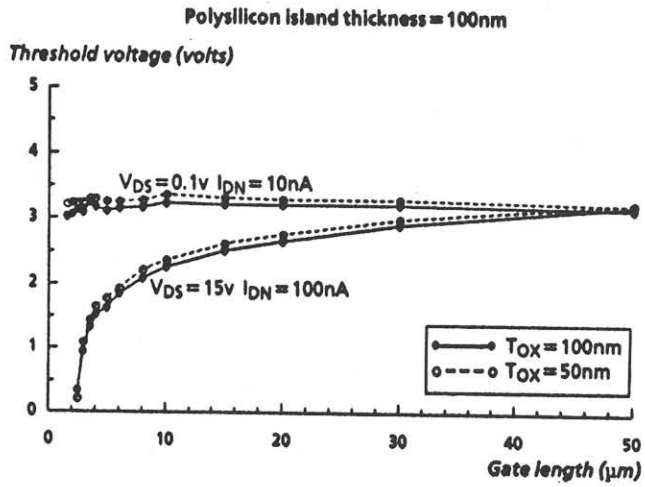

Fig. 6. Hydrogenated N-channel TFT Thresholds

8. DYNAMIC PERFORMANCE

The dynamic behavior of p-Si devices has been studied by fabricating ring oscillators and shift registers[11]. The maximum clock frequency for error free data transfer in dynamic shift registers, as a function of supply voltage, is shown in Fig. 7. It is clearly seen that, for both high temperature and low temperature processes, the performance of the shift registers at moderate supply voltages is well in excess of that required for self-scanning of a 2000 line display with 60 Hz frame frequency.

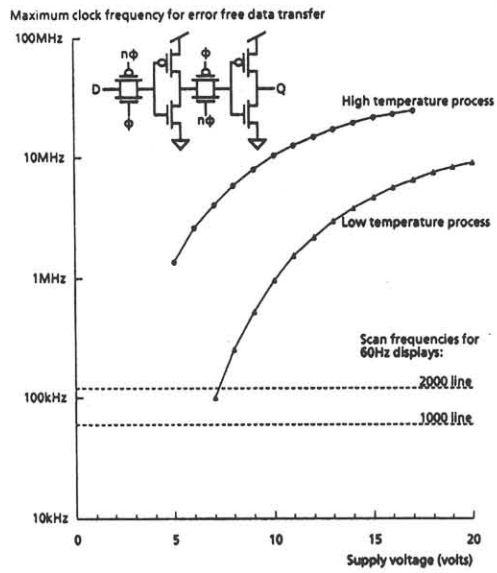

Fig. 7. Polysilicon TFT CMOS Shift REgister Maximum Speeds. Dynamic shift registers, L = 10μm, W = 30μm for all TFTs

9. ANALOG CIRCUITS

The integration of analog functions in large p-Si devices has been studied by Lewis et al[11,12]. The, so-called, kink effect is observed at high drain bias, as the electric field in the pinch-off region becomes large enough to cause impact ionization (see Fig. 8). High output impedance is essential in analog circuits, so the kink effect presents a major problem. Offset drain structures can be used to increase breakdown voltages, but at the expense of additional

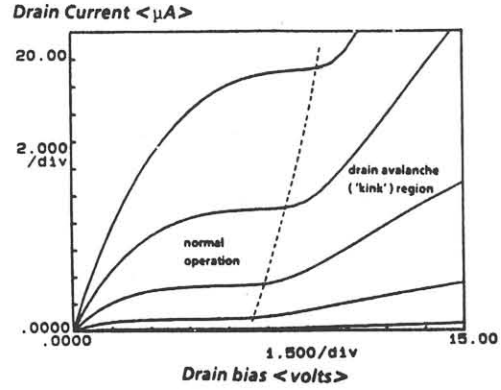

Fig. 8. N-channel poly TFT characteristics showing kink effect

processing and degraded drive current. A circuit solution using two TFTs in the cascode mode has been found to be more effective. Fig. 9 shows the frequency response[12] of a polysilicon TFT CMOS operational amplifier. The circuit uses the NMOS code structure to suppress the kink effect, and a complimentary source follower output stage to improve drive current. The success of these circuit techniques in overcoming the limitations of the TFTs can be seen in the large low frequency gain and the high bandwidth, even with large capacitive loads. For comparison, the frequency response of a single-state single crystal operational amplifier is also shown; this circuit has been built in a conventional 2μm CMOS technology and is used in a 2.5 μs conversion time analog-to-digital converter. The polysilicon TFT amplifier, although physically much larger, has higher low frequency gain and similar bandwidth to the single crystal device.

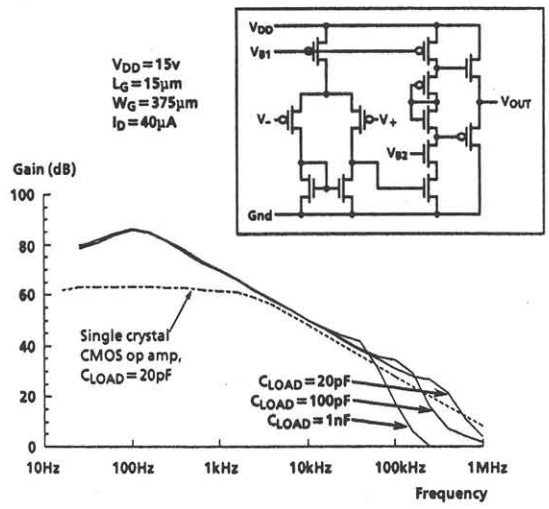

Fig. 9. Polysilicon TFT CMOS Operational Amplifier

10. CONCLUSION

Amorphous silicon devices have reached a maturity which enables their incorporation in large area arrays. They have a relatively simple structure and are particularly suitable for high voltage applications.

Polysilicon devices are somewhat less mature, but offer distinct advantages in speed and drive current, enabling good circuit performance. The process technology needs to be further developed for large area applications.

11. REFERENCES

1) H. Tuan, et al; *MRS Proc.* 33 (1984) 247-257.
2) A. Chiang, et al; *MRS Proc.* 106 (1987) 305-310.
3) I. Wu, et al; *JAP* 65 (1989) 4036-4039.
4) I. Wu, et al; *IEEE EDL* 11 (4) (1990) 167-170.
5) M. Hack, et al; *MRS Proc.* 118 (1988) 207.
6) T. Chuang, et al; *SID Digest* (1990) 508-511.
7) I. Wu, et al; *SID Digest* (1990) 307-310.
8) I. Wu, et al; *IEEE EDL* 10 (3) (1989) 123-125.
9) R. Martin et al; *IEDM* (1989) 341-344.
10) A. Lewis, et al; *IEDM* (1989) 349-352.
11) A. Lewis, R. Bruce; *ISSCC* (1990) 222-223.
12) A. Lewis, et al; *IEDM* (1988) 266-267.