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High Mobility Poly-Si TFTs Using Solid Phase Crystallized a-Si Films Deposited by Plasma Enhanced Chemical Vapor Deposition

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Thin film transistors (TFTs) have been developed on quartz substrates by using large grain size polycrystalline silicon (poly-Si) films. The poly-Si films were fabricated by solid phase crystallization (SPC) of amorphous silicon (a-Si) deposited by plasma enhanced chemical vapor deposition (PECVD). We have found that crystallinities of the SPC poly-Si are strongly correlated with the TFT characteristics especially with TFT mobilities. The TFT mobility can be enhanced substantially up to $158cm^2/Vs$ by SPC of the PECVD a-Si.

1. INTRODUCTION

Poly-Si TFTs have attracted much attention in recent years because they have broad applications to liquid crystal displays (LCDs)[1] and linear image sensors[2]. High mobility poly-Si TFTs, which allow the production of high performance LCDs or image sensors with on-board peripheral circuits and load elements in static random access memories (SRAMs), have been extensively studied.

Various approaches to achieving high mobility poly-Si with large grains, such as solid phase crystallization (SPC) and laser annealing of a-Si, have been widely studied. In particular, SPC has the advantages of mass production over the laser annealing technique. Several studies have been reported on the SPC of a-Si deposited by low pressure chemical vapor deposition (LPCVD)[3], rf sputtering, and Si ion implantation[4].

We have developed TFTs with poly-Si films crystallized from a-Si films[5]. The a-Si was deposited by PECVD because PECVD is able to make uniform a-Si films on large area substrates. This paper discusses the SPC processes of the a-Si films and examines the TFT device qualities in correlation with the crystallinities of the SPC poly-Si films.

2. EXPERIMENTAL PROCEDURE

Poly-Si TFTs were processed as follows. Intrinsic a-Si films were deposited on quartz substrates by conventional PECVD. Rf power density was $63mW/cm^2$ operated at 13.56MHz rf discharge. A SiH_4 and H_2 gas mixture with a total gas flow rate of 100sccm and gas pressure of 0.8torr was used for the deposition. Substrate temperature was maintained at 180°C during deposition and the film growth rate was 4.2Å/sec. Deposited a-Si film thickness was 1500Å. The as-deposited a-Si films contain approximately 8 atomic per cent of bonded H atoms, which was determined by infrared absorption technique. In order to remove the H atoms which may suppress the SPC-growth, the a-Si films were annealed in N_2

atmosphere at 450°C for 30 minutes before the SPC growth. Then the SPC growth was carried out at three different annealing temperatures: 600, 650, and 700°C in N_2 atmosphere. Annealing time was varied from 1 to 72 hours. Gate insulators were formed by thermal oxidization of the poly-Si at 1150°C in O_2 atmosphere. The oxide layer was 1200Å. Gate electrodes were formed with doped poly-Si deposited by LPCVD on the gate insulators. Source and drain regions of the TFTs were formed by ion implantation. Channel width is 10 µm. Channel length L of the n- channel and p-channel TFTs are 6µm and 5µm, respectively. Finally, TFTs were passivated by hydrogen to reduce trap densities at grain boundaries of the SPC-grown poly-Si.

The structures of the SPC-grown poly-Si were observed by transmission electron microscopy (TEM). Crystallinities of the poly-Si were measured by Raman spectroscopy and X-ray diffraction. Electron spin resonance (ESR) and secondary ion mass spectrometry (SIMS) were also used to determine the poly-Si film properties.

3. RESULTS and DISCUSSIONS

TEM micrographs of the SPC-grown poly-Si subjected to 600, 650, and 700°C annealing are shown in Figure 1. The SPC at 600°C for 8 hours generates crystalline nuclei of approximately 1µm which serve as seeds in an amorphous matrix (Fig.1(a)). Dendrite-shape grains larger than 2µm are obtained by the SPC at 600°C for 17 hours, although an amorphous phase region still remains (Fig.1(b)). The amorphous region changes to crystalline phase with 72 hours SPC at 600°C (Fig.1(c)). The SPC at 650°C generates crystalline nuclei within 1 hour annealing (Fig.1(d)) and changes amorphous regions to poly-Si within 2 hours

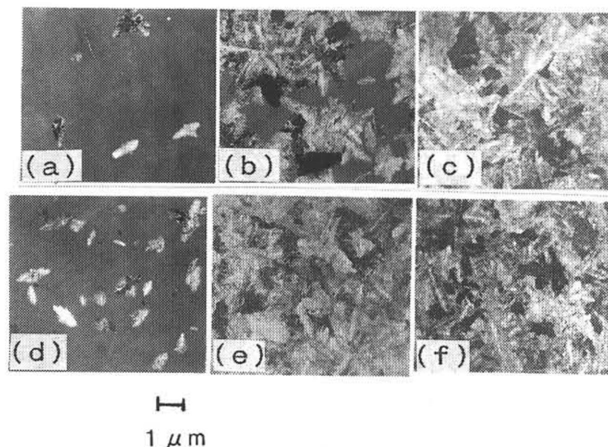

Fig.1 TEM micrographs of Si films for various annealing conditions
(a) 600°C 8h. ; (b) 600°C 17h. ;
(c) 600°C 72h. ; (d) 650°C 1h. ;
(e) 650°C 2h. ; (f) 700°C 1h ..

(Fig.1(e)). In the case of the 700°C SPC, amorphous-to-crystalline phase transition occurs within 1 hour annealing (Fig.1(f)). These results indicate that polycrystalline nucleus generation density becomes less when annealed at lower temperature.

Raman spectra of the SPC-grown poly-Si obtained by 600°C annealing are shown in Figure 2. The Raman spectrum of the Si film without annealing shows a broad peak at $480cm^{-1}$, which corresponds to an amorphous

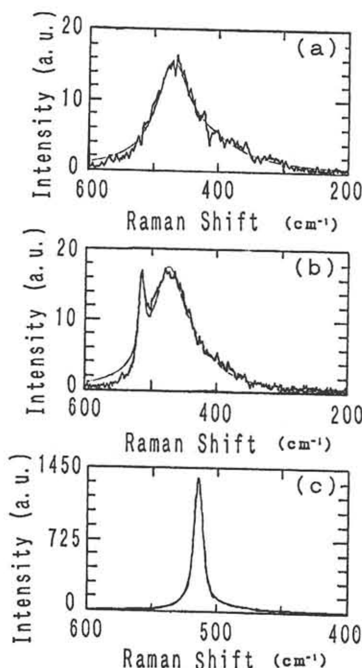

Fig.2

Raman spectra of the SPC Si films annealed at 600°C
(a) 0 h.
(b) 8 h.
(c) 72 h.

phase. The spectrum of the SPC poly-Si with 8 hours annealing shows two peaks: a broad peak at 480 cm^{-1} and a sharp peak at 517 cm^{-1} which corresponds to crystalline phase. The spectrum of poly-Si with 72 hours annealing shows a single sharp peak at 517 cm^{-1}, which indicates that the amorphous-to-crystalline phase transition has occurred. Figure 3 shows X-ray diffraction intensities of the SPC poly-Si as a function of the annealing time. X-ray diffraction intensity, which is the summation of (111), (220), and (311) signals, increases with lower annealing temperature and longer annealing time. These results also show that the lower annealing temperature requires longer annealing time to generate crystalline nuclei in an amorphous matrix. In particular, it is noted that the SPC at 600°C requires a fairly long incubation time of 8 hours to generate the crystalline nuclei.

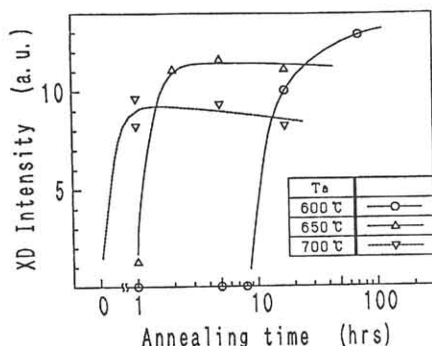

Fig.3 X-ray diffraction (XD) intensities of the SPC Si films as a function of the annealing time at varied annealing temperature Ta.

To examine the origin of the above incubation time, we have measured electron spin density and hydrogen concentration of the SPC films. Figure 4 shows relationships between electron spin density and H concentration of the SPC poly-Si annealed at 600°C. Sample annealing time is denoted beside each measured point in fig.4.

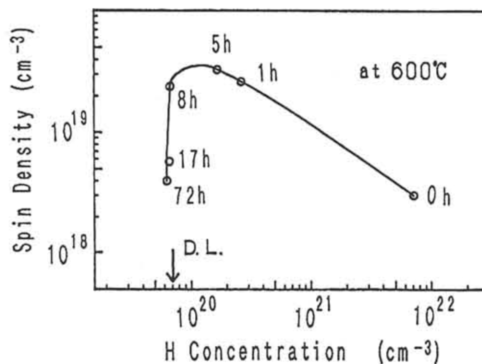

Fig.4 Electron spin density vs. hydrogen concentration of the SPC Si films annealed at 600°C. The annealing time is noted beside each measured point. The arrow indicates the lower detection limit of hydrogen concentration (D.L.).

Electron spin density and H concentration were measured by ESR and SIMS, respectively. The detection limit of H concentration in the SIMS measurement is approximately 7×10^{19} cm^{-3}. Annealing up to 5 hours releases hydrogen in the film, which results in increasing spin density. Then H amount decreases below the detection limit during 5 to 8 hours annealing, while spin density in turn slightly decreases. For over 8 hours annealing, spin density rapidly decreases. Referring to the above result as well as TEM, Raman and X-ray measurements, we postulate the following process. Initial annealing up to 5 hours dissociates hydrogen in the film generating dangling bonds. The hydrogen dissociation is required before generating crystalline nuclei. Annealing between 5 to 8 hours further dissociates hydrogen and starts recrystallization, which results in a decreasing number of dangling bond. The number of dangling bond rapidly decreases with annealing over 8 hours because recrystallization proceeds.

Figure 5 shows typical subthreshold characteristics of TFTs fabricated with the SPC poly-Si annealed at 600°C for 72 hours.

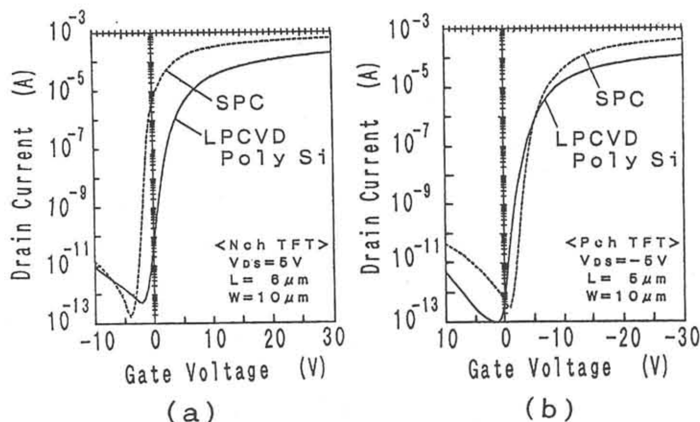

Fig.5 Subthreshold characteristics of the TFTs. (a) n-channel; (b) p-channel.

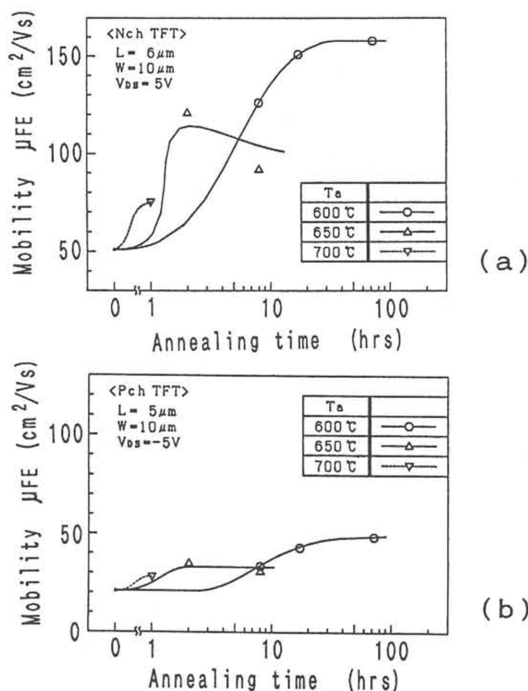

Fig.6 The field effect mobilities of the SPC TFTs as a function of the annealing time at varied annealing temperature Ta. (a) n-channel; (b) p-channel.

Fig.5(a) shows the n-channel TFT, and Fig.5(b) shows the p-channel TFT. Dotted lines denote the curves of the SPC-TFTs, and solid lines denote the curves of TFTs using poly-Si deposited by LPCVD without the SPC. The field effect mobility of the n-channel and the p-channel SPC TFTs are 158cm^2/Vs and 49cm^2/Vs, respectively. An ON/OFF current ratio of 10^9 has been achieved.

Figure 6 shows the field effect mobilities of the TFTs as a function of the SPC annealing time. Fig.6(a) shows the n-channel TFT while Fig.6(b) shows the p-channel TFT. With reference to the TEM observation, the Raman spectra, and the X-ray measurements, we conclude that the high degree of crystallinity of the SPC poly-Si results in higher field effect mobility.

4. CONCLUSION

We observe substantial increase of the TFT mobilities by using SPC of PECVD a-Si. The field effect mobilities of the TFTs were approximately a factor of 10 times higher than those of the LPCVD poly-Si TFTs. These results indicate that the TFTs have adequate performance for application to the peripheral circuit of LCDs, image sensors, SOI structures, and 3-dimensional integrated circuits.

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REFERENCES

1) S.Morozumi: SID Seminar Lecture Note, vol.2, May 19 (1989) 10/1.
2) M.Kunii, K.Hasegawa, H.Oka, Y.Nakazawa, T.Takeshita and H.Kurihara: IEEE Trans. Electron Devices, vol.36, No.12 (1989) 2877.
3) T.Aoyama, G.Kawachi, N.Konishi, T.Suzuki, Y.Okajima and K.Miyata: J. Electrochem. Soc., vol.136, No.4, (1989) 1169.
4) K.T.-Y.Kung and R.Reif: J. Appl. Phys. vol.62, No.4, (1987) 1503.
5) S.Takenaka, H.Oka, R.Takenaka, T.Takeshita and H.Kurihara: Extended Abstracts (The 50th Autumn Meeting, 1989); The Japan Society of Applied Physics, No.2, 553.