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# Low Temperature Poly-Si TFT's with Various Source/Drain Processing Techniques

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High quality poly-Si TFT's have been made using a low temperature (630 °C) process with a conventional MOS structure. The characteristics are substantially improved by the use of a TOMCATS silicon oxide gate insulator. On the other hand, a 'modified sintering' process results in an enhanced H-passivation effect.
Alternatives for ion implantation have been successfully investigated. Highly conductive Source and Drain regions were realized by a selective 'poly-epitaxial' growth technique resulting in a self-aligned process.

## 1. INTRODUCTION

Thin film transistors (TFT's) on transparent substrates are very important for active matrix type Liquid Crystal Displays (LCD's). The peripheral driving circuits can also be integrated when poly-Si TFT's are used due to the higher field effect mobility compared to amorphous silicon TFT's. Since large areas are required, low cost substrates are inevitable. Therefore, the maximum processing temperature of the TFT's should not exceed 650 °C. High quality low temperature poly-Si can be obtained by thermal recrystallization of LPCVD amorphous Si[1)2)].

Silicon oxide made by APCVD of $SiH_4$ is the most classical gate insulator used in poly-Si TFT's. However, it has moderate electrical properties. Alternatives such as sputter-deposited $SiO_2$[3)] or double layer structures[4)] have been proposed. In this work, we use the second approach. A thin, dry thermally grown polyoxide was formed which was subsequently covered by a TOMCATS $SiO_2$. This oxide is formed from the organic precursor tetramethylcyclotetrasiloxane (TMCTS or TOMCATS - $Si_4C_4O_4H_{16}$).

In this work, the use of H-plasma passivation at the end of the TFT process is avoided, since the latter requires an additional step. Instead, H-passivation is realized by a 'modified sintering' technique of the Al contacts.

Ion implantation is commonly used in the standard processing for Source and Drain formation of poly-Si TFT's. However, ion implantation technology may not be suitable for large area processing. Therefore, novel techniques such as laser doping from the gas phase[5)] or from the solid phase[6)] and low energy ion shower doping[7)] are under world-wide investigation. In this paper, we present the use of P-doped poly-Si Source and Drain that can be deposited by standard rf-PECVD deposition equipment.

## 2. EXPERIMENTS

Poly-Si TFT's were made on borosilicate glass (HOYA NA-40), quartz and oxidized wafers with a conventional MOSFET structure. Firstly, an amorphous Si film with a thickness of 100 to 300 nm was deposited by LPCVD at 550 °C. The films were annealed at 630 °C in $N_2$ during 3 hrs. for recrystallization. Then, a thin polyoxide was formed at 630 °C in dry $O_2$ during 10 hrs., followed by the definition of the active areas. We compared the classical $SiO_2$, made by APCVD from $SiH_4$, to $SiO_2$ made by LPCVD from TOMCATS. The TOMCATS $SiO_2$ is deposited in a commercial horizontal-tube

LPCVD reactor. The thickness uniformity is very good (± 2% over a 5" area) and it has a very conformal step coverage. A 100 nm thick $n^+\mu C$-Si film was deposited by PECVD to form the gate electrode. After definition, the devices were implanted by P or B at a dose of $5.10^{15}$ cm$^{-2}$ to form Source and Drain. The activation of the dopants was done by a 5-hours anneal at 630 °C in $N_2$. Then, a 500 nm thick APCVD $SiO_2$ field insulator was deposited by APCVD from $SiH_4$, followed by the definition of the contact holes. The metallization consists of 1 µm of Al deposited by e-gun evaporation. On some samples the metal layer was patterned <u>before</u> the sintering ('normal sintering'). However, on some samples the patterning was performed <u>after</u> the sintering ('modified sintering'). The sintering was done at 435 °C in F. G. for 20 minutes. Alternatively, a 100 nm Ti / 1 µm Al layer was used for metallization, without sintering.

## 3. RESULTS AND DISCUSSION

### 1) Double gate insulator

Table I gives an overview of the typical TFT characteristics : subthreshold slope (S), threshold voltage ($V_{th}$), and field-effect mobility ($\mu_{fe}$). The channel length and width varies between 10 and 80 µm.

One denotes the beneficial effect of the TOMCATS gate insulator compared to the classical APCVD $SiO_2$. Indeed, table I shows a substantial increase in $\mu_{fe}$ and decrease in S and $V_{th}$. It is speculated that TOMCATS has a lower density of interface states. The effect of the thin polyoxide is almost negligible. Spectroscopic ellipsometry and XTEM reveal that the thickness is only 2 nm.

### 2) H-passivation

It is known that sintering of the Al contacts releases atomic hydrogen. The H passivates the dangling bonds at the grain boundaries and at the bulk/gate interface thereby improving the TFT quality[8]. In this work, a 'modified sintering' was applied to perform the H-passivation. A larger amount of hydrogen can be generated by doing the sintering <u>before</u> the patterning because of the larger volume of Al present at the moment of the sintering. Indeed, in table

| sintering | | | no | normal | modified |
|---|---|---|---|---|---|
| gate insulator | APCVD | S(V/dec.) | 4.3 | 2.0 | 1.35 |
| | | $V_{th}$ (V) | 37 | 16 | 8 |
| | | $\mu_{fe}$(cm$^2$/Vs) | 14 | 30 | 38 |
| | TMCTS | S(V/dec.) | | 1.6 | 1.05 |
| | | $V_{th}$ (V) | | 12 | 5 |
| | | $\mu_{fe}$(cm$^2$/Vs) | | 40 | 56 |

Table I: Influence of the type of silicon oxide gate insulator and way of sintering on the poly-Si TFT performance. The poly-Si thickness is 180 nm.

I an important improvement of $\mu_{fe}$, $V_{th}$ and S can be seen, compared to the 'normal sintering'.

By combination of the 'modified sintering' together with the use of a TOMCATS gate insulator, high quality n-channel poly-Si TFT's have been realized : $\mu_{fe}$ = 41 cm$^2$/V.s, $V_{th}$ = 6 V, S = 0.9 V/dec and $I_{on}/I_{off} > 10^6$ (fig.1). Even higher $\mu_{fe}$ are obtained when using a thicker bulk layer : for 180 nm respectively 300 nm bulk layer thickness the $\mu_{fe}$ equals 56 cm$^2$/V.s respectively 72 cm$^2$/V.s. This is attributed to the larger grain size. From SEM analysis a grain size of 0.35 µm respectively 0.5 µm is determined for a 100 nm respectively 300 nm thick poly-Si layer.

P-channel poly-Si TFT's were also made. Fig.2 shows a $\mu_{fe}$ = 35 cm$^2$/V.s, $V_{th}$ = -15 V, S = -1.5 V/dec and $I_{on}/I_{off} > 10^6$ for a 100 nm thick poly-Si bulk layer. No dependence on channel length and width is observed both for n-channel and p-channel.

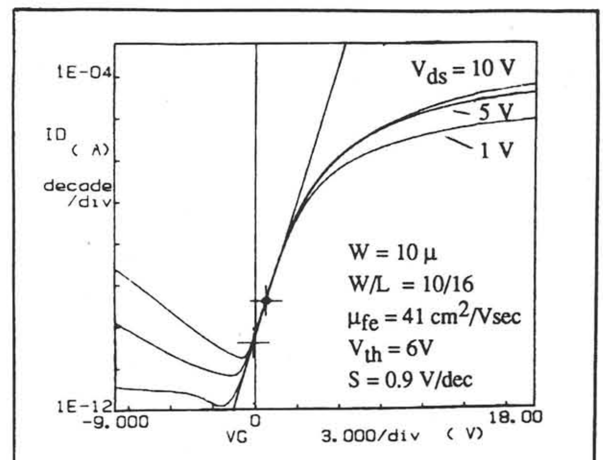


Fig.1: Drain current - gate voltage characteristics of low temp. n-channel poly-Si TFT with TOMCATS gate insulator. The poly-Si thickness is 100 nm.

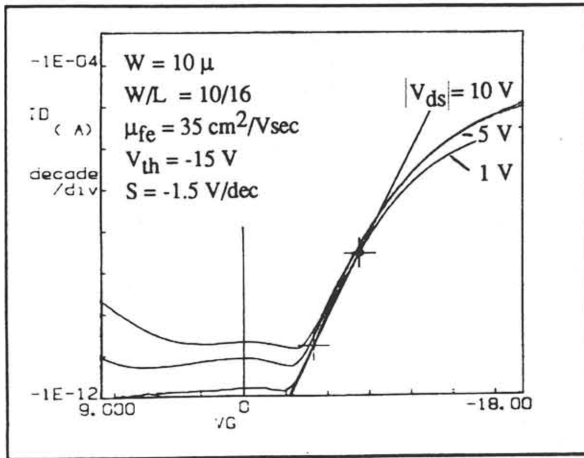


Fig.2 Drain current - gate voltage characteristics of low temp. p-channel poly-Si TFT with TOMCATS gate insulator. The poly-Si thickness is 100 nm.

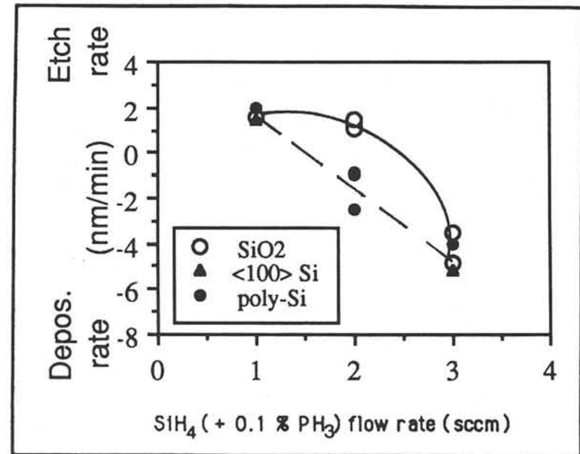


Fig.3: Etch and deposition rate of Vapour Phase Epitaxy films on c-Si, poly-Si and SiO2. Selective deposition is obtained as a balance between etching and deposition.

3) Highly conductive Source and Drain deposited by RF-PECVD techniques

In previous work, we have demonstrated that large-grain P-doped poly-Si with a resistivity down to $10^{-3}$ Ohmcm is deposited when rf-PECVD epitaxial growth technique is applied to poly-Si thin films ('poly-epitaxy')[9]. The resistivity of 'poly-epitaxial' P-doped poly-Si films is sufficiently low for poly-Si TFT applications. However, the process flow of staggered poly-Si TFT's made by this technology[1] uses an extra mask step as compared to when ion implantation is used. This is because ion-implantation allows self-aligned Source and Drain formation. Therefore, we now developed selective (poly-)epitaxy of P-doped Si.

For selective growth, one has to etch Si-nuclei from $SiO_2$ before they reach a critical size. We have realized selectivity by balancing plasma etching (from $SiF_4$-generated species) with plasma deposition (from $SiH_4$-generated species). The selectivity of the growth is controlled by controlling the $SiH_4$ vs. $SiF_4$ flow rate (fig.3). At low $SiH_4$ flow rate, etching occurs on all substrates. At high $SiH_4$ flow rate, non-selective growth is observed. In between, selective growth is realized. The details of this growth technique will be published elsewhere.

TFT devices have been made with P-doped Source and Drain made by non-selective and selective poly-epitaxy. The devices are similar to the ones described in par. 2, except for the fact that a 200 nm APCVD oxide was used as the gate insulator. The 5-mask (non-self-aligned) process flow used in case of non-selective growth was the same as described before[1]. The 4-mask (self-aligned) process flow when using selective deposition is shown in fig.4. After the definition of the gate insulator, P-doped poly-Si is deposited at the Source, Drain and Gate, but not on the substrate (quartz or thermal oxide) or gate oxide sidewall. Table II lists the resistivity and minimum reverse leakage current of the devices. Although the P-content of both types of P-doped poly-Si films is comparable (1-2 %), the selectively deposited poly-Si films have a resistivity about one decade higher. This is attributed to the lower activation efficiency of P in the selectively deposited films. In terms of reverse leakage current, the selective growth process is at present slightly inferior to ion implantation or non-selective growth. Further research will focus on lowering the resistivity and leakage current.

## 4. CONCLUSIONS

High quality poly-Si TFT's are realized by using poly-Si made by thermal recrystallization of LPCVD amorphous Si. The maximum process temperature is 630 °C and the process is successful both for n and p-channel devices. A TOMCATS $SiO_2$ layer is a strong candidate to be used as gate insulator in low temperature poly-Si TFT's. On the other hand, an

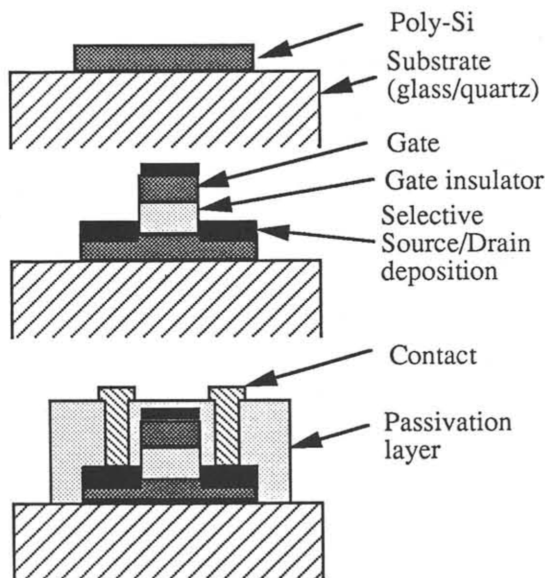


Fig.4: Process flow for self-aligned TFT with Source and Drain deposited by selective 'poly-epitaxial growth'

| | Poly-Si grain-size ≤ 40 nm | Poly-Si grain-size 100-300 nm | |
|---|---|---|---|
| Source/Drain deposition: | R (Ohm.cm) | R (ohm.cm) | I (A) |
| Vapour Phase Epitaxy | 6E-3 | / | / |
| Selective Vapour Phase Epitaxy | / | 2E-2 | 4E-11 |
| Solid Phase Epitaxy | 4E-3 | 2E-3 | 8E-12 |

Table II: Resistivity R, and minimum reverse leakage current I ($V_{ds}$= 5V, W/L = 10/10) for poly-Si TFT' s with different grain-size and different Source/Drain deposition technology.

efficient H-passivation can be obtained by means of a 'modified sintering'.

A selective 'poly epitaxial' growth technique has been demonstrated in a rf-PECVD deposition equipment. It results in highly conductive Source and Drain regions still maintaining a self-aligned process.

5. ACKNOWLEDGEMENTS

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REFERENCES

1) K.Kobayashi, J.Nijs and, R.Mertens; J.Appl. Phys.65(1989) 2541
2) A.Mimura, N.Konishi, K.Ono, J.Ohwada, Y.Hosokawa, Y.Ono, T.Suzuki, K.Miyata, and H.Kawakami; IEEE Trans. Electron Devices, vol.ED-36(1989) 351
3) T. Serikawa, S.Shirai, A.Okamoto, and S.Suyama; Jpn.J.Appl. Phys.28(1989) L 1871
4) A.Mimura, T.Suzuki, N.Konishi, T.Suzuki, and K.Miyata; IEEE Electron Device Lett., vol.EDL-9 (1989) 270
5) P.Coxon, P.Lloyd, and P.Migliorato; Appl. Phys. Lett.48(1986) 1785
6) T.Sameshima, S.Usui, and H.Tomita; Jpn.J.Appl. Phys.26(1987) L1678-1680
7) A.Yoshida, M.Kitagawa, K.Setsune, and T.Hirao; Ext. Abstr. of the 20th SSDM Conf., Tokyo, Japan (1988) 109-112
8) M.Rodder, and D.A.Antoniadis; IEEE Electron Device Lett., vol.EDL-6(1985) 570
9) K.Baert, P.Deschepper, H.Pattyn, A.Rodriguez, J.Nijs, and R.Mertens; Thin Solid Films 184 (1990) 139