

Low Thermal Budget Poly-Si Thin Film Transistors on Glass

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A new low thermal budget fabrication process for polycrystalline silicon thin film transistors (TFT's) on 7059 glass is presented. This processing incorporates low temperature crystallization by rapid thermal annealing (RTA) of low temperature plasma enhanced chemical vapor deposited (PECVD) a-Si:H, the use of high quality gate oxide deposited at 200°C, and extremely short time hydrogen passivation using an electron cyclotron resonance (ECR) source. These TFT's, produced with this processing, were found to have mobilities in the 60 cm²/v-sec range. The subthreshold slope of these devices was in the 1 volt/decade range and the threshold voltage was around 5 volts.

This paper surveys the three key processing steps, crystallization of a-Si, gate oxide deposition, and hydrogenation passivation, that form the core of a fabrication process that yields low thermal budget, high quality poly-Si thin film transistor(TFT) structure on glass. The characteristics of these TFT's fabricated using this processing are then shown and discussed.

We use a-Si:H on 7059 glass as the precursor material for the poly-Si because our earlier work⁽¹⁾ showed that RTA crystallization of such low temperature PECVD a-Si:H films could result in much larger grains than those attainable from crystallizing or recrystallizing LPCVD materials for the same thermal budget. In addition, that earlier work showed that this large grain material could be attained on glass at low thermal budgets. In the TFT results we report here, the precursor PECVD a-Si:H was deposited at 250°C and then crystallized using thermal budgets ranging from 650°C to 700°C for 50 to 5 min. The thickness of the a-Si:H films was 2000Å and the grain size after crystallization on the 7059 glass was typically 1µm. This low thermal budget crystallization also served to activate the dopants in

the source /drain regions. The source /drain regions were implanted prior to crystallization using P implants at a dosage of 2x10¹⁵ cm⁻² at 40 KeV.

After crystallization, low temperature reactive magnetron sputtering was used to deposited the gate dielectrics. The gate oxide used was SiO₂. Several different approaches have been reported^(2,3) for depositing gate SiO₂; however, many of them need high temperature processing to obtain a high quality oxide. We were able to obtain, however, a suitable oxide by magnetron sputtering from an SiO₂ target in an O₂ and argon mixture ambient. The oxygen to argon ratio was 1:1 at a total gas pressure of 2 mtorr. During this magnetron sputtering, the substrate was held at 200°C. We note that the etching rate of this magnetron sputter deposited SiO₂ film in 1:100 HF:H₂O was 40Å/sec which may be compared to 30Å/sec for thermally grown SiO₂ or for 900°C LPCVD SiO₂, and to 60 Å/sec for 450°C LPCVD SiO₂.

The hydrogen passivation step in this processing involved using our electron cyclotron

resonance (ECR) source. Our previous comparative studies^(4,5) have shown that ECR hydrogenation of polycrystalline Si is superior to that provided by an rf hydrogen plasma or a Kaufman hydrogen source. The superiority is simply not just due to that fact that ECR can offer a higher dose, but, more importantly, it is due to the fact that ECR provides more effective species for the passivation. Our TFT's were passivated in an ECR hydrogen source at 300°C for 5 or 15 min. The pressure and the power on the ECR system were 1.2×10^{-4} torr and 600W, respectively.

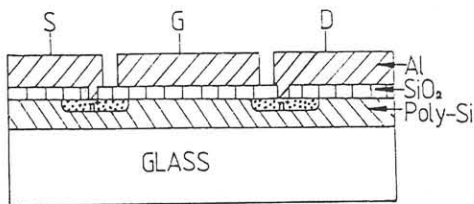


Fig.1 The structure of the TFT's

The TFT's used in this study had a conventional coplanar structure as shown in Fig.1. The gate width of these devices was $75 \mu\text{m}$ and the gate length ranged from $7.5 \mu\text{m}$ to $25 \mu\text{m}$. The drain current as a function of the source and gate voltage of these devices before and after ECR hydrogen passivation were shown in Fig.2. These data are for TFT's fabricated using our typical condition, 700°C and 5min annealing. The mobility of these TFT's before ECR hydrogenation was $20 \text{ cm}^2/\text{v}\cdot\text{sec}$. This mobility was measured when the gate and the drain were tied together and biased at 13 to 15 volts. This relatively high mobility before the passivation was due to the large grain size which was obtained by using our unique RTA crystallization approach, and due to the high SiO_2/Si interface quality. We believe that the use of O_2 ambient during crystallization is responsible for the quality of the SiO_2/Si interface. That is, a thin SiO_2 layer is actually thermally grown on the poly-Si film during the crystallization, and this thin thermally grown SiO_2 layer dominates the quality of the SiO_2/Si interface. The mobility was increased

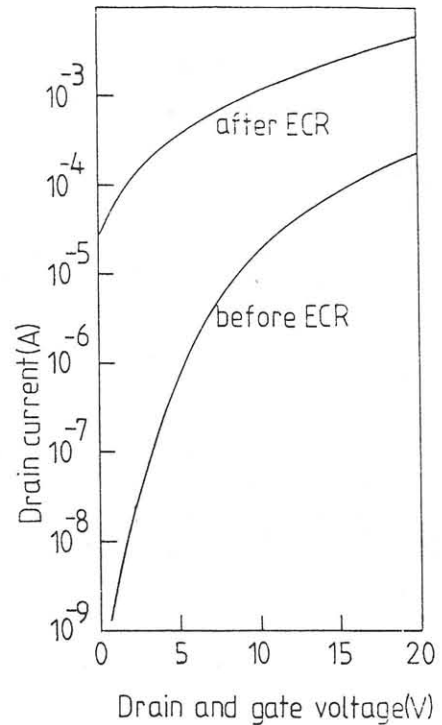


Fig.2 Drain and gate voltage vs. drain current

further to $60 \text{ cm}^2/\text{v}\cdot\text{sec}$ by subsequent ECR hydrogenation, which, we believe, passivates the defects at grain boundaries and at the SiO_2/Si interface.

In conclusion, low thermal budget poly-Si TFT's were successfully fabricated on 7059 glass substrates. The large grain poly-Si film was obtained by using a low thermal budget RTA process. No peel-off and pinholes were found on these crystallized films under a microscope. The gate SiO_2 was achieved by using magnetron sputtering system at 200°C . These TFT's, produced with this processing, were found to have mobilities in the $60 \text{ cm}^2/\text{v}\cdot\text{sec}$ range. The subthreshold slope of these devices was in the 1 volt/decade range and the threshold voltage was around 5 volts. In addition the devices were very stable. The approach introduced in the paper could be used for a large area device fabrication such as that needed for flat panel displays.

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REFERENCES:

(1) G. LIU, S. J. FONASH; Appl. Phys. Lett. 55(7). (1989)660.

(2) JUN-ICHI OHWADA, et al; IEEE Trans. Electron. Devices vol36 (1989)1923.

(3) TAKASHI NOGUCHI, et al; Jpn. J. Appl. Phys. 24 (1985)L434.

(4) R. A. DITIZIO, G. LIU and S. J. FONASH; Appl. Phys. Lett. 56(12) (1990)1140.

(5) R. A. DITIZIO, G. LIU and S. J. FONASH, to be published

