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HF Surface Passivation Failure in Integrated Thermal Oxidation Processing

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Ultraclean, integrated MOS oxide fabrication has been investigated for the first time by combining (i) surface cleaning in inert ambient , (ii) wafer transfer through ultrahigh vacuum, and (iii) thermal oxidation in a UHV-based rector. Device-quality oxide structures are obtained under suitable conditions, while under other circumstances chemical mechanisms severely degrade electrical performance: even in ultraclean environments, impurity-related silicon (Si) etching reactions before oxidation degrade oxide quality, but this can be avoided by appropriate use of passivating oxide films which prevent roughness associated with etching.

Future ULSI technology will have to rely on improved control of contamination and will have to realize steps to simplify process sequences for increased yield and reduced turn-around time. Integrated processing equipment is increasingly used to achieve the necessary control of transfer and processing ambients to reduce contamination. An element missing so far in this integrated processing direction is the development of a fundamental understanding of the requirements for optimal processing ambients and wafer passivations. We have constructed an integrated processing equipment[1] with in-situ surface analysis to address specifically those issues. The integration of surface cleaning with analysis without air exposure between the two steps allows unambiguous characterization of the as-cleaned surfaces, and a correlation with electrical figures of merit of simple, in-situ processed device structures (MOS capacitors). Si(100) wafer pre-clean followed by thermal oxide growth has been successfully integrated and conditions for surface passivation leading to good MOS capacitor characteristics have been defined.[2]

1. EXPERIMENTAL AND RESULTS

3.25" diam. Si(100) wafers have been cleaned using different cleaning methods:

(a) RCA clean[3] as control,

(b) diluted HF dip clean,

(c) HF vapor clean,

(d) H_2O_2 clean,

(e) UV-ozone[4] clean.

As cleaned wafers were loaded under inert, highly purified atmosphere, pumped to ultrahigh vacuum (UHV) conditions, and the state of the surface was analyzed using techniques such as X-ray photoemission spectroscopy (XPS). HF treated wafers were found to be essentially free of oxide and hydrocarbon contamination, but terminated with a layer of adsorbed hydrogen[5] (evidenced by high resolution electron energy loss spectroscopy - HREELS). H_2O_2 and UV-ozone treated wafers are terminated with a thin oxide layer (~1 nm thick). Thermal desorption spectroscopy (TDS) indicates that the hydrogen passivation after HF exposure is removed from the wafer surface after anneal

to 500°C leaving the Si surface exposed[6] (Figure 1), whereas the thin oxide remains intact up to temperatures well above 800°C.

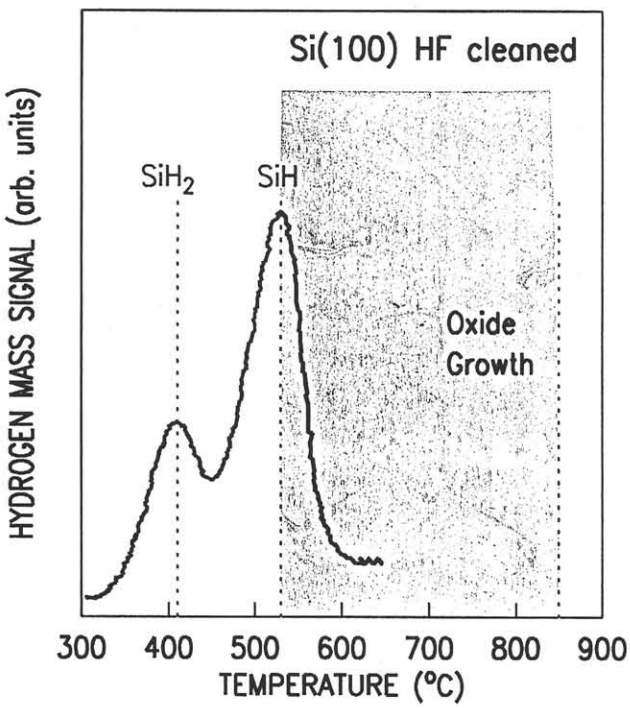

Fig. 1: Thermal desorption spectrum of HF-dip cleaned sample. Ramp-rate was 10°C/sec. Hydrogen desorption is shown for m/e=2. Peak desorption temperatures are 410°C for SiH_2 surface species and 535°C for SiH surface species. The oxidation temperature of 850°C is indicated. The shaded area indicates the temperature range at which the silicon surface is clean and exposed to reaction with trace impurities.

Subsequent to the pre-clean, wafers were loaded under UHV conditions into the UHV-compatible oxidation reactor (base pressure 10^{-8}torr). The wafers were ramped up to temperature after the reactor had been vented with either ultra-pure Ar or oxygen. Thermal oxidation was performed at 850°C to grow ~12 nm SiO_2. Some wafers were preannealed for 10 minutes in ultrapure Ar at the process temperature of 850°C. After oxidation the wafers were removed from the system and Al dots were deposited on the oxide. A breakdown statistics of wafers cleaned with the standard RCA clean is compared to breakdown statistics of wafers after initial HF and UV-ozone clean in Figure 2. Both the control wafer (RCA cleaned) and the UV-ozone cleaned wafer show good breakdown fields (~13 MV/cm), in contrast to the HF cleaned wafer that shows very poor breakdown (≤5 MV/cm). This results suggests that a thin oxide present prior to oxidation is crucial for obtaining high quality gate oxides in an integrated processing system. It also demonstrates that integration of the proper pre-clean and thermal oxide growth can yield MOS structures with very good breakdown characteristics.

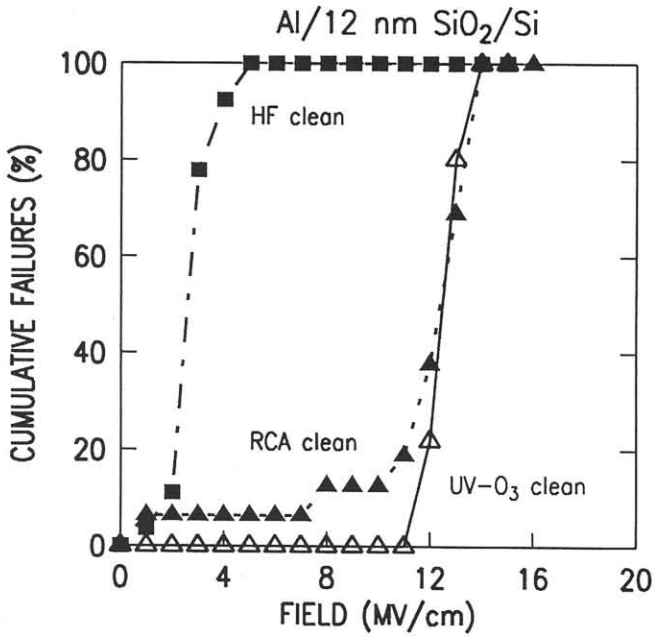

Fig. 2: Cumulative breakdown statistics for integrated preclean and oxidation treatments, cf. control.

Ramping the wafer up to process temperature in an oxidizing ambient instead of an inert ambient always gave rise to good

breakdown statistics of the thin oxide. It is only for ramp-up to temperatures above ~700°C in an inert ambient containing trace amounts of impurities (ppm - ppb of H_2O or O_2) that the quality of the thin oxide is significantly deteriorated. Smith and Ghidini[7] have shown that sufficiently low concentrations of O_2 at elevated temperatures cause etching of the surface rather than oxidation due to the formation of volatile SiO. The statistical nature of the etching reaction leads to roughening of the surface prior to oxidation with obvious consequences for the breakdown behavior due to field enhancement at interfacial asperities[8].

Evidence for the roughening of the interface is presented in Figure 3, which shows cross-sectional transmission electron microscope pictures of $Si/SiO_2/polySi$ structures pre-cleaned with HF vs. UV-ozone. Surface roughening due to etching of the bare Si surface occurs only on the HF cleaned surface because the surface passivation layer (hydrogen) desorbs in that case at temperatures well below the process temperature (see Figure 1). This leaves the surface exposed to the deleterious effect of reaction with trace impurities (H_2O, O_2). In contrast, a thin oxide film will persist during an anneal to process temperatures of ~850°C thereby protecting the Si surface against the etching reaction.

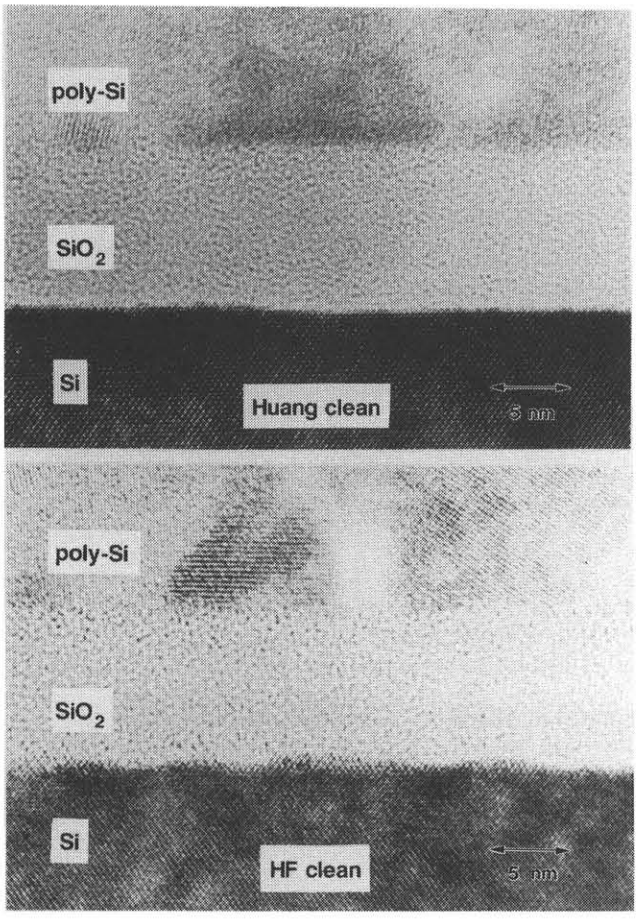

Fig. 3: Cross-sectional transmission electron microscope pictures of $Si/SiO_2/polySi$ structures, where the Si surface had been pre-cleaned with HF or RCA-clean prior to thermal oxidation.

ACKNOWLEDGEMENTS

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