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Hot Carrier Effects in nMOSFET at 77 K and 300 K

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Hot carrier effects in nMOSFETs were investigated at 77K and 300K. When supply voltage is less than 1.5V, substrate current is smaller and device life time is longer at 77K than those at 300K. It is found that this phenomenon is caused by lower equilibrium electron energy at 77K and by non-steady state transport effects. 77K operation is one of the promising approaches for realizing higher speed and more reliable scaled down MOS ULSIs.

1. INTRODUCTION

A low temperature MOSFET has been studied extensively because of its higher performances, such as steeper subthreshold slope and higher transconductance. Due to lower phonon scattering rate which increases carrier energy, and due to lower detrapping probability, hot carrier effects are believed to be one of the most serious problem for low temperature operation. However, a recent experiment shows that when V_d<2V, substrate current is smaller at 77K than at 300K[1,2]. This seems to suggest lower carrier energy at 77K. However, there has not yet been a sufficient explanation for this phenomenon. Furthermore, few reports are available on the relationship between I_{sub} and device degradation at 77K, and reliability at low temperature is still questionable.

In this paper, substrate current and device degradation characteristics of conventional nMOSFETs at 77K and 300K are investigated experimentally and theoretically in terms of carrier energy.

2. EXPERIMENTAL

The experimental devices were conventional n-channel MOSFETs with n^+ poly-Si gate. Oxide thickness and effective channel length were in the range of 55-195Å and 0.25-1.95μm, respectively. Surface boron concentration was about $10^{17}cm^{-3}$. Conventional arsenic doped single drain structure was used, because LDD (lightly doped drain) structure can not be used at 77K due to carrier freezeout effect in n^- region.

DC stress tests were carried out at maximum substrate current condition, which leads to maximum degradation for both 77K and 300K. Device life time was defined as the time for 10% transconductance degradation.

3. RESULTS AND DISCUSSION

3.1 SUBSTRATE CURRENT CHARACTERISTICS AT 77K

Fig. 1 shows typical I_{sub} characteristics of nMOSFET with T_{ox}=55Å and L_{eff}=0.55μm. When both V_d and V_g are higher than 1.5V, I_{sub} is always larger at 77K than at 300K. However, when V_d and V_g are lower than 1.5V, I_{sub} is smaller at 77K than at 300K. This phenomenon was observed in all devices measured.

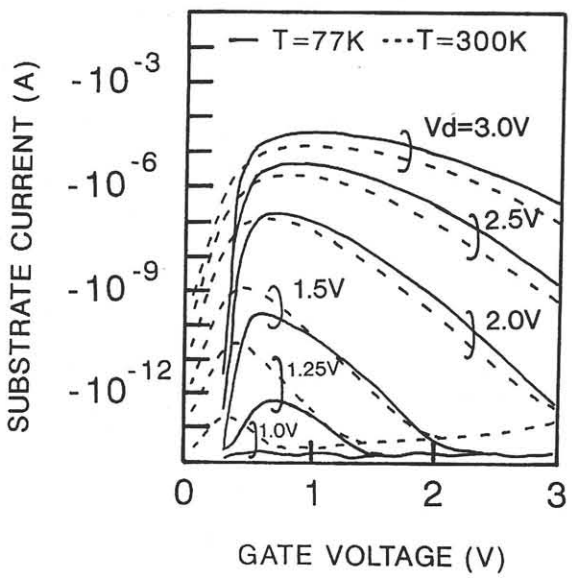

Fig. 1 Substrate current characteristics measured at 77K and 300K for nMOSFET with T_{ox}=55Å and W_{eff}/L_{eff}=45μm/0.55μm. When supply voltage is lower than 1.5V, I_{sub} at 77K is lower.

Substrate current is generated by impact ionization at drain edge. Hence, impact ionization coefficient (α), which is approximately proportional to I_{sub}/I_d, is used for discussion. According to conventional impact ionization model, α depends on local electric field because it is generally assumed that electrons reach steady state at any point in MOSFET. However, as shown in Fig.2, electric field is rapidly changing in the high field region near the drain edge. Therefore, it is expected that I_{sub} characteristics is influenced by non-steady state effects. In this case, α doesn't depend on local electric field but depends on local average carrier energy. Then, a 2D device simulator, METRO[3], which contains carrier energy transport model, was utilized for investigating the I_{sub} characteristics.

Fig. 3 shows average electron energy (w) distribution along the electron path obtained by METRO. When V_d=1.25V and V_g=0.5V, the maximum average electron energy, which determines I_{sub}, is lower at 77K than at 300K, although the phonon scattering rate decreases with temperature. Since thermal equilibrium is held at source edge and lateral electric field (E_l) in the channel is sufficiently low, electrons have smaller average energy at 77K than at 300K before entering the high field region. Moreover, because high field region length is too short for electrons to reach steady state, and because E_l in the high field region is moderate due to the low drain voltage, carrier heating in this region is insufficient. Thus, average electron energy just before the high field region influences for maximum average electron energy, ie, w_{max}(77K) is lower than w_{max}(300K). Heat flow to the drain also contributes to further lowering w_{max}(77K) because drain works as a heat sink. This lower w_{max}(77K) leads to lower I_{sub} at 77K than at 300K.

When V_d and V_g are high, because E_l in the channel region increases, and because channel region length is sufficiently long to reach nearly steady state, electrons already have larger average energy at 77K than at 300K before entering the high field region. Thus, w_{max}(77K) is larger than w_{max}(300K), and this result leads to that I_{sub} at 77K is higher than at 300K.

Measured I_{sub} characteristics is well explained by energy transport model.

3.2 DEVICE DEGRADATION CHARACTERISTICS AT 77K

Fig. 4 shows relationship between I_{sub}/I_d, and τI_d, where τ is device life time. When $I_{sub}/I_d > 10^{-2}$, τI_d at 77K is smaller than that at 300K under the same I_{sub}/I_d condition, i.e. under the same average carrier energy condition. This is due to lower detrapping probability of oxide trap at 77K. However, the slope of τI_d-(I_{sub}/I_d) characteristics is larger at 77K, which indicates larger τI_d under practical operation condition, i.e., $I_{sub}/I_d < 10^{-2}$ or I_{sub} per channel width is lower than 2×10^{-6}A/μm. Since I_d at 77K is only 1-2 times as large as that at 300K, larger τI_d at 77K indicates that

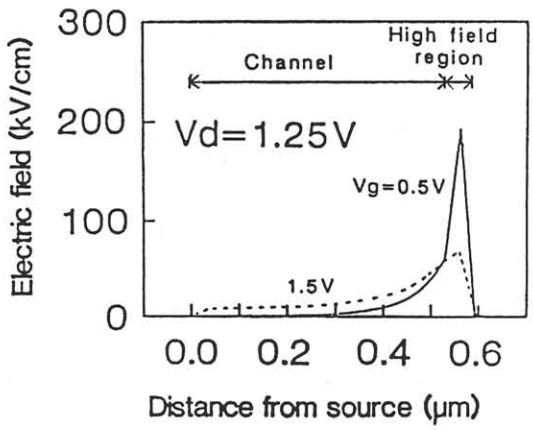

Fig. 2 Simulated lateral electric field along electron path. The bias condition is V_d=1.25V. Since electric field is rapidly changing in high field region, non-steady state effects is significant here.

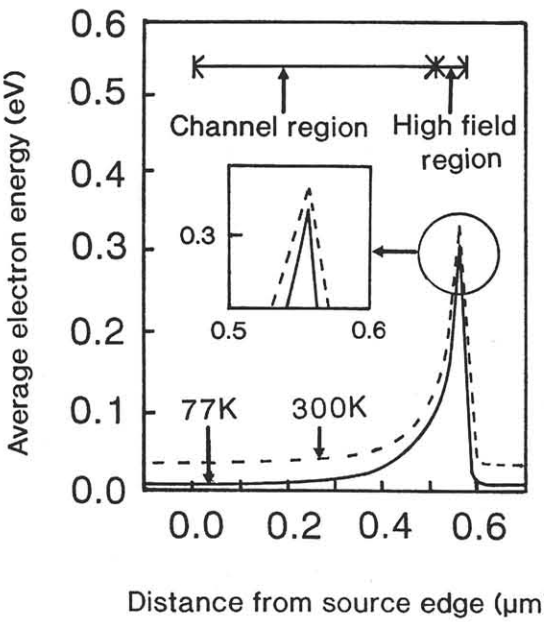

Fig. 3 Simulated average electron energy distribution along electron path. The bias condition is V_d=1.25V and V_g=0.5V. Maximum average electron energy is lower at 77K than at 300K due to lower initial energy at 77K and non-steady state effects in high field region.

device life time is longer at 77K than at 300K.

Hot electron at the **Si/SiO$_2$** interface is responsible for device degradation. On the other hand, I_{sub} is cause by the hot electron in the **bulk**, where average electron energy is maximum. Therefore, 2D electron energy distribution is important for τI_d-(I_{sub}/I_d) relation. From a simple analysis, the following modified Hu's relation is derived[4],

$$\tau I_d = A(BI_{sub}/I_d)^{-\gamma} \quad (1)$$

$$\gamma = (\phi_{it}/\phi_{th})/(w_{int}/w_{max}) \quad (2)$$

where A and B are lattice temperature dependent constant. ϕ_{it} and ϕ_{th} are threshold energy of interface state generation and impact ionization,respectively. w_{max} is the maximum average electron energy, which determine I_{sub}. w_{int} is the average electron energy at the point where degradation is most severe. This point locates near the drain edge at Si/SiO_2 interface[4]. Assuming that temperature dependence ϕ_{it} and ϕ_{th} are weak, the results of Fig. 4 indicates that the ratio of w_{int} to w_{max} is smaller at 77K than at 300K.

Fig. 5 shows 2D average electron energy distribution obtained by METRO. The bias conditions were set to give the same I_{sub}/I_d or w_{max} for 77K and 300K. As shown in this figure, w_{int} at 77K is lower that 300K, i.e. γ at 77K is smaller than at 300K. It is because of higher mobility, non-steady state effects, and lower thermal equilibrium energy at 77K. Although lower detrapping probability of the oxide trap at 77K shortens the device life time, decrease of w_{int} at 77K compensates and even surpasses the trap effect since population of the hot carrier affecting device degradation is proportional to $\exp(-\phi_{it}/w_{int})$, assuming that energy distribution is Boltzmann distribution. Thus, smaller w_{int} at 77K results in longer life time at 77K under same w_{max}, i.e. I_{sub}/I_d, when I_{sub} per channel width is lower than 2×10^{-6}A/μm.

3.3 SUPPLY VOLTAGE FOR 77K MOS LSI

The above analysis indicates that for $V_d<1.5$V, 77K operation gives smaller I_{sub} under the same bias conditions, and longer life time under the same I_{sub} conditions. Therefore, higher V_d is allowed at 77K when power supply voltage is scaled down to 1.5V or less.

4. CONCLUSION

Hot carrier effects in nMOSFETs were characterized at 77K and 300k. When $V_d<1.5$V, 77K operation reduces the degradation in MOSFET characteristics. Lower equilibrium electron energy at 77K and non-steady state electron transport are responsible for these effects. 77K operation is one of the most promising approaches for realizing higher speed and high reliability MOS ULSIs.

ACKNOWLEDGMENT

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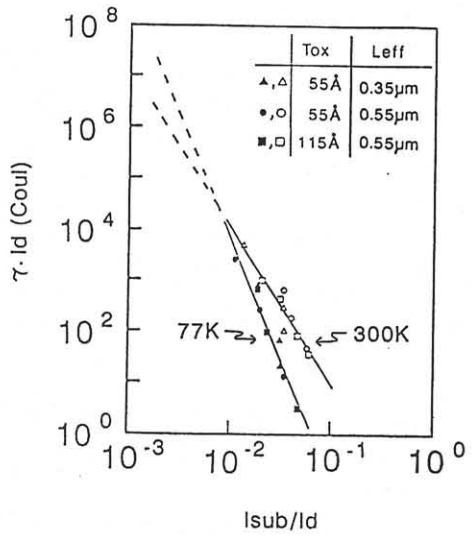
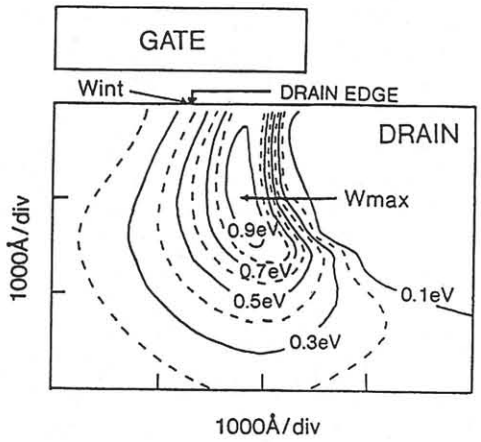
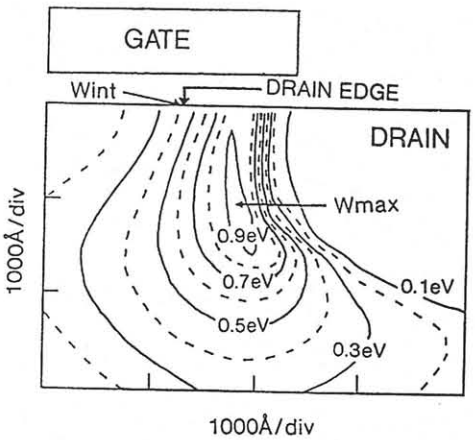


Fig. 4 Relationship τI_d vs. I_{sub}/I_d. The slope corresponds to $(\phi_{it}/\phi_{th})/(w_{int}/w_{max})$.



(a) T=77K,Vd=4.0V,Vg=1.5V



(b) T=300K,Vd=4.5V,Vg=1.5V

Fig. 5 Simulated 2D average electron energy distribution at (a)77K and (b)300K. The bias conditions are set to give same I_{sub}/I_d, i.e. w_{max} for 77K and 300K. w_{int} at 77K is lower than w_{int} at 300K.