PMOSFET Hot-Carrier Degradation Analyzed Over Ten Orders of Magnitude

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Hot-carrier degradation is measured over ten orders in time on three types of buried-channel PMOSFETs (p-channel metal-oxide-semiconductor field-effect transistors) for three oxide thicknesses at various gate- and drain voltages. No special initial-stage degradation is observed, enabling a consistent description of the degradation based on the two dominating effects. Firstly, electrons injected into the oxide cause negative oxide charge, leading to channel length reduction with a logarithmic time dependence. Secondly, holes cause interface states that reduce the transconductance with a power-law time dependence.

1. INTRODUCTION.

Hot-carrier degradation of sub-micron PMOSFETs threatens the reliability of advanced integrated circuits. Negative and/or positive oxide charge^{1,2}) and interface states generated by electrons and/or holes^{3,4}) are held responsible. HEIP (hot-electron-induced punch through) is generally accepted¹), but many ambiguities remain. For instance, logarithmic⁵) versus saturating power-law⁶) time dependence for worst-case degradation, or interface states⁷) versus positive charge²) causing degradation at more negative gate voltages. We use charge pumping to study the relevant degradation mechanisms separately.

Three buried-channel PMOSFET types are used with $t_{ox} = 6.5$, 11 and 15 nm. Only the latter type has a lightly doped drain (N_B = 5*10¹² cm⁻² at 25 keV and 25 nm spacer). Standard characteristics and charge-pumping curves are measured three times per decade (1,2,5 sequence from μ s to hrs). Degradations shorter than one second are realized by a drain voltage pulse (100 ns edges), with the d.c. voltages at the other terminals.

Using $g_{m,sq}$ and g_m (maximum transconductances at $V_D = -0.1$ V of an undegraded large square transistor and of the (degraded) transistor, respectively), we define $L_{eff} = W g_{m,sq} / g_m$, where $W = 10 \ \mu m$ is the transistor width. Charge-pumping current (I_{cp}) is measured with⁸) constant-amplitude gate pulses ($f = 500 \ \text{kHz}, \tau = 100 \ \text{ns}, \Delta V_G = 3 \ \text{V}$) at various gate-pulse base levels (V_{base}). We determine the oxide charge (N_{ox}) from its local threshold voltage (V_{cp}), defined as the highest V_{base} at which $\Delta I_{cp}(t) = I_{cp}(t) - I_{cp}(0)$ is half its (shifted) peak value. We compensate for the shifts of the I_{cp} curve due to N_{ox} when calculating the generated interface states

$$\Delta N_{SS}(t) = N_{SS}(0) * \frac{\int \Delta I_{cp}(t) d V_{base}}{\int I_{cp}(0) d V_{base}}.$$
 (1)

The maximum of $I_{cp}(0)$ determines $N_{ss}(0)$ as usual⁸).

2. CHARGE-PUMPING CURVES.

Charge-pumping measurements during two hot-carrier degradation experiments are shown in figure 1. We summarize our interpretation only, since it is described in detail elsewhere⁹). At $V_G \approx V_D$ interface state formation causes the degradation (figure 1a), whereas worst-case degradation (at maximum gate current, $I_{G,max}$) reveals simultaneous creation of negative oxide charge and inter-



Figure 1: Charge-pumping current during (a) degradations at $V_G \approx V_D$ and (b) at maximal gate current.



Figure 2: Threshold voltage near the oxide charge versus the normalized channel shortening during degradation at maximum gate current.

face states in the same part of the transistor (figure 1b). The electrons that are generated in the pinch-off region and injected into the oxide cause the negative charge¹). It attracts an inversion layer that extends the drain into the channel, resulting in channel shortening $\Delta L_{eff} < 0$.

Figure 2 shows the recently introduced⁵) damage monitor $(-\Delta L_{eff}/t_{0x})^{0.5}$ plotted versus V_{cp} , yielding straight lines with slopes proportional to t_{0x}^{-1} . Hence $\Delta N_{0x} \propto \Delta V_{cp}/t_{0x} \propto (-\Delta L_{eff}/t_{0x})^{0.5}$ for oxide charge distributed homogeneously over the oxide thickness⁹). This links the universal⁵) time dependence of $\Delta L_{eff}/t_{0x}$ to the time dependence of the oxide charge generation.

Figure 3 shows that the generated interface states at $I_{G,max}$ are strongly related to the generated oxide charge, independent of L_{eff} or V_D . This suggests that the electrons generate oxide charge and interface states in the same part of the transistor ($\Delta N_{ss} > 0$ in the shifted peak in figure 1b only) simultaneously. Degradation at $I_{G,max}$ (electron injection) of a transistor that had been stressed at $V_G \approx V_D$ proceeds identically to degradation at $I_{G,max}$ of a virgin transistor. This proves the absence of significant positive oxide charge after degradation at $V_G \approx V_D$, since no enhanced initial degradation is observed.



Figure 3: Number of generated interface states versus the channel shortening during degradation at $I_{G,max}$.

Degradation at $V_G \approx V_D$ of a transistor that had been stressed at $I_{G,max}$ reveals that, at $V_G \approx V_D$, the interface states are not caused by electrons. Both in the degraded part (right peak in figure 1b) and in the undegraded part (left peak) additional interface states are formed, showing a broad damaged area (compared with continued degradation at $I_{G,max}$), probably caused by holes.

3. TIME DEPENDENCE.

Figure 4 shows hot-carrier degradation at various gate voltages measured over ten decades in time. We do not observe noticeable initial-stage degradation of any parameter, in contradiction to the significant effects reported by Igura et al.¹⁰). During degradation at IG.max, (- $\Delta L_{eff}/t_{ox}$)^{0.5} shows a logarithmic time dependence over ten orders in time9), reflecting the time dependence of Nox generation. The logarithm may be explained by electric-field dependent charge trapping11), taking into account the reduced electric field due to the oxide charge. After long degradation (or at more negative V_G) the time dependence is changed (partially) into the well known (for NMOSFETs) power law t0.45 of interface state formation9). The reduced transconductance increases the channel length according to our definition. We introduce the time scales for interface state- and oxide charge generation, τ_{Nss} and τ_{Nox} , respectively, to fit the data in figure 4a to a combination of these degradation modes

$$\Delta L_{eff}/t_{ox} = (t / \tau_{Nss})^{0.45} - \{0.33 \log_{10}(1 + t / \tau_{Nos})\}^2.$$
(2)



Figure 4: (a) Normalized channel shortening, (b) number of interface states and (c) threshold voltage near the oxide charge versus time. The time axis is normalized on the time scale of oxide-charge related degradation.

We normalized the time axis in figure 4 on τ_{Nox} to show that the time scales of figures 4a, 4b and 4c are strongly correlated when oxide charge dominates the degradation.

Figure 4b shows two distinct processes for interface state formation, presumably related to electrons and holes. The interface state formation caused by holes has a stronger time dependence, because no negative oxide charge builds up that reduces the electric fields and⁶) the injected current (IG \propto t^{-0.4}). Even when $\Delta L_{eff}/t_{ox}$ increases due to interface states (e.g. at $V_G = -2.5$ V in figure 4a), V_{cp} (in figure 4c) still shows the logarithmic time dependence of ΔN_{ox} . Hence V_{cp} is a sound measure for ΔN_{0x} , hardly influenced by the interface states, as long as the maximum of ΔI_{cp} is in the shifted peak.

The coefficients of equation 2 and the gate- and substrate currents are plotted versus the gate voltage in figure 5a and 5b, respectively for two drain voltages.

The peaks of I_G and τ_{Nox} are at the same gate voltages, consistent with electrons causing Nox (and 'harmless' Nss). The electrons are generated by impact ionization in the pinch-off region and accelerated towards the gate. The most energetic electrons enter the gate oxide, creating the damage and forming the gate current The

peaks of I_B and τ_{Nss} occur at different gate voltages, suggesting that the mechanism is not channel-hot-hole injection. The holes probably originate from avalanche generation by the electrons of the substrate current in the large perpendicular field. These holes are accelerated towards the gate oxide outside the pinch-off region, in accordance with our observation of a broad damaged area (section 2). Both the interface state formation and the charge trapping strongly depend on the electric field in the oxide11), complicating a more detailed analysis.



Figure 5: (a) Parameters of equation (2) and (b) gateand substrate currents versus the gate voltage.

4. ADDITIONAL EFFECTS.

In addition to the two most important degradation mechanisms described in section 3, four effects may be relevant. Firstly, for too negative gate voltages, Fowler-Nordheim injection may generate additional interface states. Secondly, for strong electric fields, hole injection near the drain may generate positive oxide charge. Thirdly, below the threshold voltage, band-to-band tunneling may cause additional degradation. Finally, near V_T (in short-channel devices), a threshold voltage shift may significantly change the currents during degradation.

We checked that Fowler-Nordheim tunneling is not important in our case by performing similar experiments, but with $V_D = 0$ V, showing no serious degradation. Slight deviations (caused by positive oxide charge?) from log(t) dependence have been observed in short-channel transistors for $V_{GD} = V_G - V_D > 5$ V at $t_{ox} = 6.5$ nm and for $V_{GD} > 8$ V at $t_{ox} = 15$ nm only, minimizing their significance for normal operating conditions. Band-toband tunneling is not significant (for $V_D \approx 0$) in our transistors, eliminating the third effect. During the fourth effect, the hot-electron-induced shift of the threshold voltage enlarges the drain-, substrate- and gate currents during the degradation, instead of the decrease (caused by the oxide charge) that is observed under normal degradation conditions 6), resulting in a logarithmic time dependence with a factor larger that 0.33 in equation (2). This effect is observed clearly in our experiments at $V_G \approx$ V_T, but even this faster degradation is of limited importance, because it never reaches the level of worstcase degradation (that occurs at more negative VG).

5. CONCLUSIONS.

Hot-carrier degradation of PMOSFETs shows no special initial degradation down to 1 µs. Energetic electrons (the gate current) generate negative oxide charge and (harmless) interface states. Energetic holes generate interface states without oxide charge during normal operation. The negative oxide charge shortens the channel length logarithmically in time, whereas the hole induced interface states reduce the transconductance with a power of time. These two dominating effects suffice to interpret PMOS degradation over ten orders in time.

- M. Koyanagi et al, IEDM Tech.Dig, (1986) 722. 1)
- K.R. Hofmann, Proceedings of "Insulating Films 2) On Semiconductors", (1983) 98.
- F. Matsuoka et al, IEEE trans. El. Dev. ED-37, 3) (1990) 1487.
- P. Heremans et al, IEEE trans. El. Dev. ED-35, 4) (1988) 2194.
- R. Woltjer and G.M. Paulzen, IEDM Tech. Dig, 5) (1990) 561.
- B.S. Doyle and K.R. Mistry, 6)
- IEEE trans. El. Dev. ED-37, (1990) 1301. T, Tsuchiya and J. Frey, 7)
 - IEEE El. Dev. Lett. EDL-6 (1985) 8.
- 8) G. Groeseneken et al,
- IEEE trans. El. Dev. ED-32, (1985) 375. R. Woltjer et al, HCIS Conf, Nara, Japan, (1991) 9)
- to be published in Semicond. Science and Techn. Y. Igura et al., SSDM Tokyo, (1987) 31. 10)
- M.M. Heyns et al, Appl. Surf. Sc 39, (1989) 327. 11)