Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 14-16

Spatial Distribution of Trapped Holes in the Oxide of MOSFETs after Uniform Hot-Hole Injection

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Hole trap distribution and time dependence of charge free layer have been investigated after uniform hot-hole injection into the gate oxide of p-channel MOSFETs. It has been found that hole trap distribution has an exponential variation with respect to the distance from the Si/SiO_2 interface and exists within 6 nm from the interface. A charge free layer exists near the interface as a consequence of hole detrapping. The measured charge free layer width was found to be increasing initially with time and saturates at around 4 nm.

1. Introduction

Scaling down the size of MOSFETs for high integration of VLSI technology without reducing the supply voltage causes high electric field in the device. It often leads to the generation of hot carriers and thereby injection of these carriers into the gate oxide of MOSFET. Although the role of hot-holes in the malfunctioning of MOSFETs has long been discussed,[1-2] it is only recently that quantitative studies on hot hole injection has started. The device degradation during hot hole injection is mainly due to the trapping of injected holes in the gate oxide. So, in order to avoid possible degradation it is necessary to identify and characterize the nature and distribution of hole traps in the gate oxide.

In this study, we investigated the spatial distribution of hole traps in the gate oxide using a set of p-channel MOSFETs having very thin oxide thicknesses in the range of 4.6 to 10.6 nm. Also, the time variation of charge free layer width[3] due to detrapping of trapped holes has been analized using the experimental data of drain current measured after hot-hole injection.

2. Experimental procedure

The p-channel MOSFETs used in this study were fabricated in CMOS process with channel doping density of $5X10^{17}$ cm^{-3} and gate area of 100X100 μm^2. Gate oxide was grown at 850°C in dry oxygen. Finally, annealing was done in N_2 at 900°C for 37 minutes.

In this experiment, our aim was to observe the shift of I_d-V_g characteristics caused by hole trapping and subsequent recovery due to detrapping. To inject hot-holes, we followed the 'Injection by forward biased diode' technique.[4] Bias conditions during hot-hole injection is schematically shown in Fig. 1. Hot-holes were uniformly injected into the gate oxide for an injected hole density of 10^{14} cm^{-2} with a reverse bias applied to the n-well, together with a forward bias between the n-well and p-substrate. Voltages applied to the p-substrate and the n-well were 5.3V and 4.5V, respectively. Fig. 2 shows the energy band diagram during hot hole injection. Shift of I_d-V_g characteristics along the negative voltage axis, during hole injection was monitored periodically. The time variation of drain current due to the detrapping of trapped

holes was measured under a given bias condition for a long time (~ 6 hours) in order to observe the recovery of the threshold voltage from the maximum shift caused by trapping. During this measurement, the substrate-well junction was biased to 0 V.

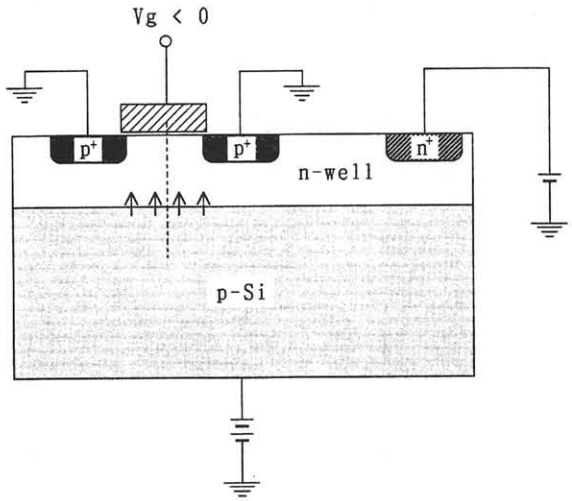

Fig.1. Schematic diagram of the MOS transistors used in the experiment with biasing voltages applied during hot-hole injection.

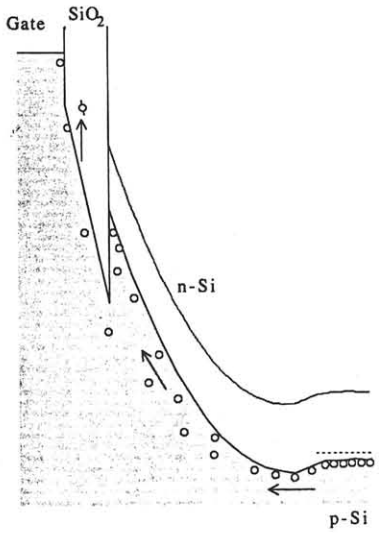

Fig. 2. Schematic view of energy band diagram during hole injection.

3. Results and Discussion

Fig. 3 shows the spatial distribution of trapped holes as obtained by deconvoluting the relation between threshold voltage shift and oxide thickness. It also illustrates the effect of oxide field on trap density.[5] During hot-hole injection, we observed parallel shift of I_d-V_g characteristics along the negative voltage axis. It demonstrates the fact that only the trapped holes instead of the interface states are responsible for the shift. Exponential trap distribution suggests that hole traps are related to structural defects located near the interface.[6,7] A charge free layer near the interface attributes to the consequence of hole detrapping. Threshold voltage recovery due to detrapping of trapped holes, towards the initial value, has been calculated using the experimental data of drain current, measured after the injection of hot-holes. Fig. 4 shows the calculated threshold voltage recovery in logarithmic time scale.

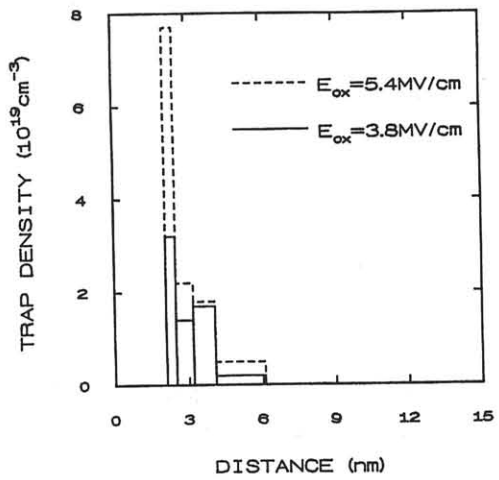

Fig. 3. Trap distribution as a function of distance from the Si/SiO_2 interface for E_{ox}=3.8MV/cm and 5.4MV/cm.

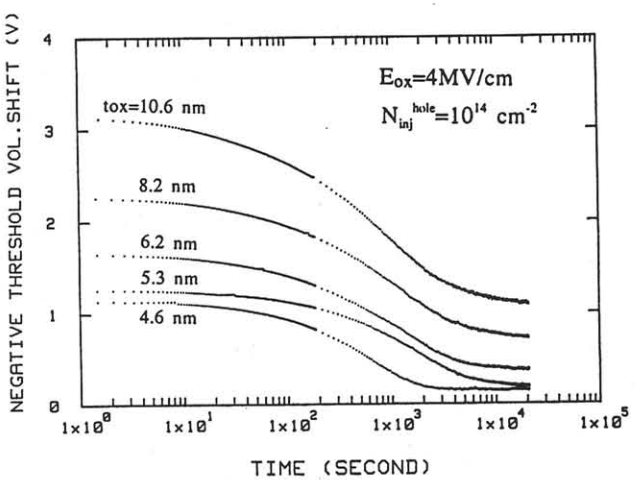

Fig. 4. Calculated data of threshold voltage recovery due to detrapping of the holes trapped in the oxide.

The width of charge free layer was derived from the relation between threshold voltage shift and gate oxide thickness at a given time as illustrated in Fig. 5. Intercept at the horizontal axis gives the width of charge free layer.[3] It should be noticed that the charge free layer at 10 second is different from that at 10000 sec. Fig. 6 represents the time dependence of charge free layer plotted against logarithmic time scale. It has been found that the charge free layer increases initially with time and saturates at around 4 nm. Logarithmic time dependence of the charge free layer demonstrates that hole detrapping takes place through tunneling process.[6,7]

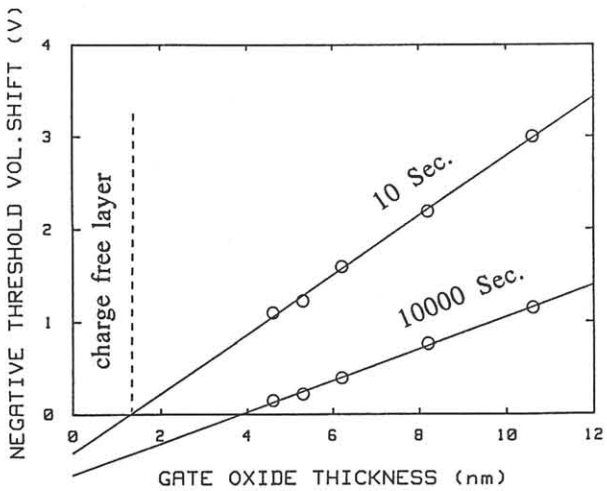

Fig. 5. Threshold voltage shifts for experimental p-MOSFETs of different oxide thickness at 10 sec. and 10000 sec. after hot-hole injection.

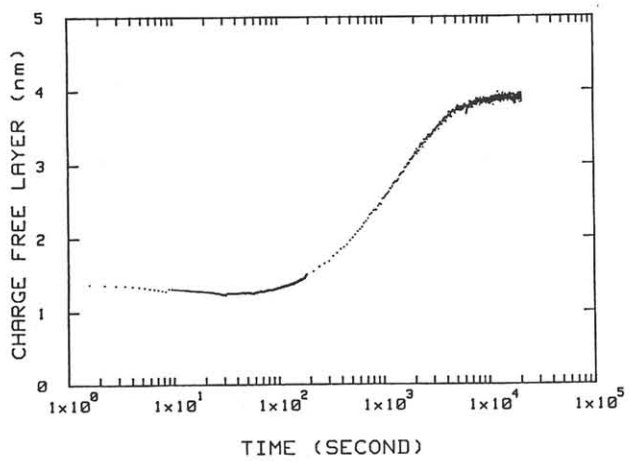

Fig. 6. Calculated time dependence of charge free layer width. Variation is shown in logarithmic time scale.

4. Conclusions

Hole trap distribution in p-channel MOSFETs having very thin oxide thickness was studied by homogeneous hot-hole injection into the oxide in a manner analogous to substrate hot-electron injection.[4,8-10] Trap distribution and time dependence of charge free layer width were measured for the first time. These were determined by analyzing the experimental data of drain current, measured after injecting some fixed number of holes. Trap distribution was found to have the shape of an exponential function with respect to the distance from the Si/SiO_2 interface, while charge free layer showed an exponential time variation before reaching saturation. Trap density has an increasing tendency with gate oxide field and exponential hole trap distribution exists within 6 nm from the Si/SiO_2 interface.

Acknowledgements

The authors would like to pay sincere thanks to Dr. K. Iguchi, Sharp Corporation for providing the experimental samples.

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