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The Influence of Synchrotron X-Ray Damage on Hot-Carrier-Induced Degradation in Subquarter-Micron NMOSFETs

T. Tsuchiya, M. Harada, K. Deguchi, and T. Matsuda

NTT LSI Laboratories
3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-01, JAPAN

Hot-carrier reliability due to residual damage in the gate oxide created by synchrotron X-ray irradiation is investigated for subquarter-micrometer NMOSFETs. Although irradiation-induced interface-traps are completely eliminated after 400 °C post-metalization- annealing, neutral electron traps partially remain. The effect of the residual traps on hot-carrier degradation can be negligible when gate oxides thinner than about 5 nm are used. It is found that there is no effect of irradiation damage on interface-trap generation during hot-carrier-injection.

1. INTRODUCTION

Synchrotron radiation (SR) X-ray lithography is promising for fabricating future deep-submicrometer ULSIs. However, there is a great concern over hot-carrier (HC) reliability due to residual damage in the gate oxide created by X-ray irradiation. Several projects have investigated the influence of the damage on HC-induced MOSFET degradation [1]-[3]. These projects have dealt with greater than half-micrometer devices with gate oxides thicker than 10 nm, and with relatively small (10^2 mJ/cm^2) maximum irradiation doses. This paper focuses on the irradiation and HC-effects for subquarter-micrometer NMOSFETs with thinner gate oxides under a wider irradiation range (10-3,000 mJ/cm^2).

2. EXPERIMENTAL PROCEDURES

N^+ poly-Si-gate NMOSFETs with 3.5-12.0 nm thick gate oxides and 80 nm deep source/drain junctions[4] were used in this study. Gate layers were patterned by EB lithography. After gate electrode fabrication, samples were annealed at 900 °C for 30 minutes in N_2 atmosphere to eliminate EB damage. Except for the gate layer, optical lithography was used. Irradiation experiments were performed in an NTT SOR Facility [5]. In order to investigate irradiation-induced damage and the effect of post-metalization-annealing, which is the final annealing through fabrication process, direct exposure was made without any resist layer either before or after the final annealing in N_2/H_2 forming gas at 400 °C for 30 minutes. X-ray wavelengths ranged from 0.7-1.2 nm. The maximum irradiation dose (3,000 mJ/cm^2) was set to evaluate irradiation effects due to five- or six-lithography-level exposure using typical-sensitivity X-ray resist, assuming a three-level metal process where high-temperature annealing is not performed except for the final N_2/H_2 annealing.

3. RESULTS AND DISCUSSION

3.1. IRRADIATION DAMAGE

X-ray exposure generates interface-traps, positive charges and neutral traps in the gate oxide [6]. Generated interface-traps were evaluated by charge pumping current I_{cp} [7], and they are completely eliminated after the final annealing, even under a maximum dose of 3,000 mJ/cm^2, as shown in Fig. 1. Generated positive charges also disappeared after the annealing. This was confirmed by a comparison with MOSFET characteris-

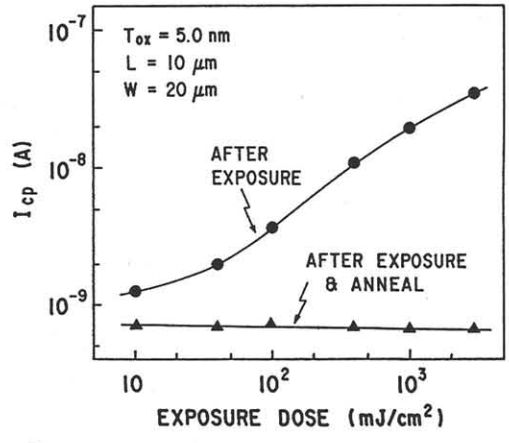

Fig. 1
Charge pumping current vs. exposure dose.

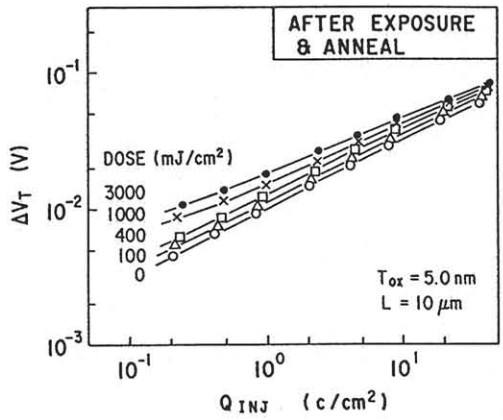

Fig. 2
ΔV_T vs. charges of electrons injected from substrate Q_{INJ}.

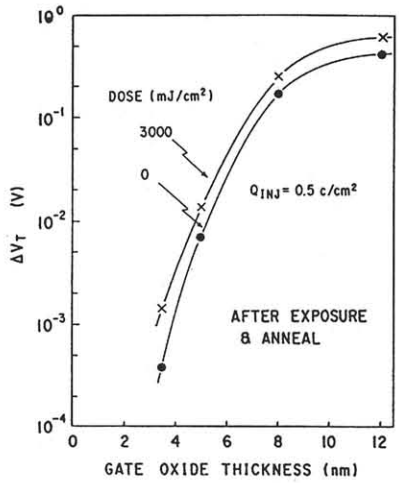

Fig. 3
Effect of gate oxide thickness on ΔV_T due to substrate hot-electron injection. L_g=10 μm.

tics of non-irradiated devices. Residual neutral traps were evaluated by threshold voltage shift ΔV_T after substrate hot electron injection [8]. ΔV_T due to the trapping of electrons are shown in Fig. 2 as a function of injected electron charges. ΔV_T increases with the increase in the exposure dose, and it cannot recover to the non-irradiated level, even after the final annealing. This means that neutral traps are not completely recovered even after the final annealing. Effects of the gate oxide thickness on ΔV_T are shown in Fig. 3 for non-irradiated devices, and for 3,000 mJ/cm^2-irradiated and subsequently-annealed devices. Injected electron-charges are fixed at 0.5 c/cm^2. ΔV_T dramatically decreases as the gate oxide thickness T_{OX} decreases below 8 nm. T_{OX} will be a key parameter in reducing the influence of the residual neutral traps on HC-degradation.

3.2. HOT CARRIER DEGRADATION

3.2.1. EFFECTS OF X-RAY DAMAGE

In order to investigate the effect of X-ray damage on HC-induced device degradation in subquarter-micrometer NMOSFETs, threshold voltage shift ΔV_T and the increase in I_{cp} dependences upon stress gate voltage under fixed stress-drain-voltage were measured. The bias-stress was applied to the devices after exposure. The results for 0.2 μm NMOSFETs are shown in Fig. 4. Compared with non-irradiated devices, ΔV_T increases remarkably with increased exposure dose, especially in the higher stress-gate-voltage range. It should be noted that ΔI_{cp} is not dependent on the exposure dose, which means that irradiation-induced damage does not play any role in interface-trap generation during HC-injection. The increase in ΔV_T is clearly due to the trapping of injected-hot-electrons in the irradiation-induced traps.

Here, it has been reported that HC-degradation is significantly increased in PMOSFETs due to the enhanced electron trapping in the oxide by the residual traps [9]. Recently, it was found that HC-degradation mode for quarter-micrometer level PMOSFETs is quite different from previous reports (i.e., effective channel-length reduction due to trapped electrons), and the new degradation mode is caused by interface-traps generated by hot-hole-injection [10]. Interface-trap generation is a more important phenomenon than electron trapping for future PMOSFETs. Therefore, the fact that there is no irradiation-induced damage effect on interface-trap generation during HC-injection is highly significant.

3.2.2 EFFECTS OF ANNEALING AND GATE OXIDE THICKNESS ON DEVICE LIFETIME

ΔV_T and ΔI_{cp} dependences upon stress gate voltage for 3,000 mJ/cm^2-irradiated and subsequently-annealed 0.2 μm-NMOSFETs are shown in Fig. 5. For comparison, those for non-irradiated devices are also shown in the figure. Gate oxide thickness for both types of devices is 5 nm. It can be seen that there are no meaningful differences in ΔV_T and ΔI_{cp} between the two types of devices. The influence of X-ray damage on HC-degradation seems to disappear after the final annealing. In order to investigate the effect of the final annealing in detail, DC device lifetimes τ were obtained as a function of substrate

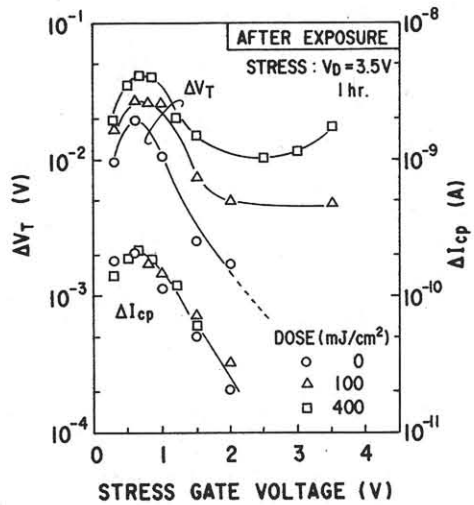

Fig. 4
ΔV_T and ΔI_{cp} vs. stress gate voltage. L_g=0.2 μm, T_{OX}=5 nm.

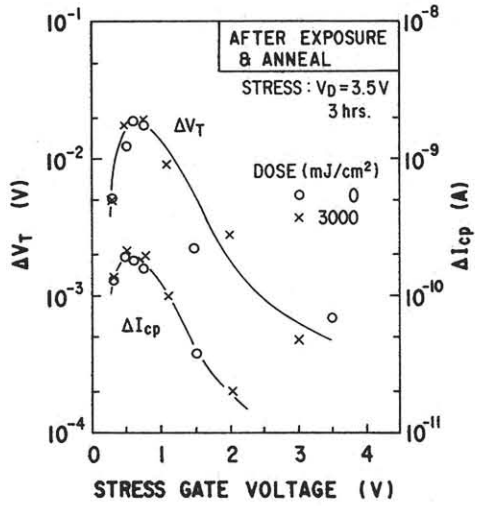

Fig. 5
ΔV_T and ΔI_{cp} vs. stress gate voltage. L_g=0.2 μm, T_{OX}=5 nm.

current normalized by channel width I_{SUB}/W_{eff}. τ is defined as time required to reach ΔV_T=10 mV. The results are shown in Fig. 6 for 0.2 μm NMOSFETs with gate oxide thickness and exposure dose as parameters. Although τ is slightly reduced due to the enhanced electron trapping for 8 nm gate oxide in higher exposure doses, there is little irradiation effect on τ for 5 nm gate oxide even at 3,000 mJ/cm^2.

Therefore, the influence of synchrotron radiation X-ray lithography on HC-induced degradation in 0.2 μm NMOSFETs is considered negligible when gate oxides thinner than about 5 nm are used, even when three-level metal processing is assumed.

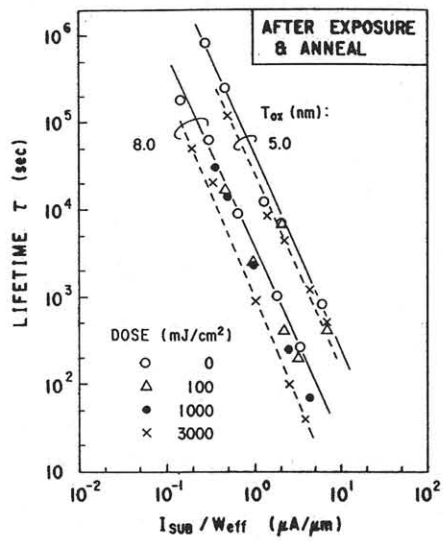

Fig. 6
DC device lifetime τ vs. I_{SUB}/W_{eff}. L_g=0.2 μm.

4. CONCLUSIONS

Synchrotron-X-ray-induced interface-traps are completely eliminated after 400 °C N_2/H_2 annealing. However, neutral traps partially remain even after the annealing. The residual damage effect on HC-degradation is negligible for subquarter-micrometer NMOSFETs when gate oxides thinner than about 5 nm are used. It was found that there is no irradiation damage effect on interface-trap generation during HC-injection. This phenomenon will be very important for deep-submicrometer PMOSFETs where HC-degradation is mainly caused by interface-trap generation, not by electron trapping in the oxide.

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