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Silicon Nanoelectronics: The Road Less Travelled

T. P. Smith, III
IBM Research Division, Thomas J. Watson Research Center
Yorktown Heights, NY 10598 USA

The study of nanometer-scale devices has attracted a great deal of attention in the past few years. A number of discoveries have heightened scientific interest in this area. There is also a great deal of interest from the technological point of view. This interest arises on both the primary (new device concepts) and the secondary (impact on existing devices) levels. Except in isolated instances, the unique potential of silicon-based materials have not been exploited to study mesoscopic phenomena. We will examine the key breakthroughs in mesoscopic physics and exploratory silicon technology that may provide extraordinary opportunities to investigate nanometer-scale electronic devices.

We would like to address the future work emerging in mesoscopic physics and nanoelectronics and its potential technological impact. In addressing this several overriding assumptions must be made. The first issue is what technology base will launch nanoelectronics. The most obvious and most likely scenario is that silicon technology will continue to dominate computation, logic, and memory. Nanometer scale transistors and circuits employing devices with sub-100nm gate lengths have already been fabricated and studied in silicon. The leading edge of semiconductor product miniaturization is being driven by memory (DRAM in particular) and the conflicting requirements of scaling and macroscopic charge storage may provide an opportunity to exploit new schemes such as single-electron circuits. In fact, a major breakthrough or innovation is probably needed for chips to store more than a gigabit of information.

Another important issue is the operating temperature for future circuits. While there are clear technological advantages associated with low-temperature (77K) operation of conventional CMOS circuits there are numerous questions regarding cooling and packaging. This is ominous since the most optimistic projections for nanoelectronics require low temperatures and in some cases cryogenic (4.2K) temperatures. We must assume that nanoelectronics alone will not drive technology to low-temperature operation and CMOS must get there first.

The final issue is the type of physics that can be used effectively for technology. We assume at this point that the leading contenders are charge quantization, spatial quantization, and resonant tunneling. There are a number of recent examples of semiconductor nanostructures that demonstrate these types of physics and might be precursors to a nanoelectronics technology: Quantum-dot capacitors, Coulomb-blockade transistors, and resonant-tunneling diodes. Each of these has been studied using III-V structures but only give a hint of what might be possible for future silicon-based devices. Based on our assumptions concerning the future of nanoelectronics and the physics that emerges at these length scales it is critical to examine developments in silicon technology to determine the likelihood of translating mesoscopic physics into novel technology.

The single-transistor memory cell is beginning to face scaling limitations. The amount of charge required for reliable storage of information cannot be reduced much beyond present levels (about 150 fC). This complicates further reduction of memory cell size since voltages continue to drop, demanding increasing capacitance. We have studied quantum-dot capacitors extensively to investigate spatial quantization. Quantum dots represent a new class of electronic structures where the electronic configuration and degree of confinement can be tuned at will. These structures mimic many atomic effects with a tremendous degree of flexi-

bility. They can be tuned from isolated to coupled quantum dots simply by changing the bias on a patterned gate. Three distinct regimes can be examined in this way: a superlattice regime; a tight-binding regime; and an isolated-quantum-dots regime.[1)]

Quantum dots also have intriguing magnetic properties. The presence of an external magnetic field couples effects of the magnetic flux with the electrostatic potential depending on the strength of the potential modulation. In strongly-coupled quantum wires and quantum dots, the commensurability between the superlattice period and the cyclotron orbit is reflected in a modification of the envelope of the magnetocapacitance oscillations. In weakly-coupled quantum dots, a new structure is observed. Aperiodic oscillations in the density of states are related to fractal-like behavior in the energy dispersion relation first predicted by Hofstadter. In completely isolated quantum wires or quantum dots, the Landau-level magnetocapacitance oscillations are recovered with a Zeeman bifurcation of the states produced by the interplay of magnetic and spatial quantization.[2)]

Another important observation is that random impurity distributions and imperfections in large arrays of quantum dots do not obscure the underlying spatial quantization. This is still somewhat puzzling but it demonstrates that spatial quantization of electrons can be detected and even averaged without losing the discrete nature of the process. While numerous questions still remain, one can envision schemes where the total charge required for reliable information storage could be reduced by exploiting discrete quantum-state effects.

Recent work by Mierav, Kastner, and Wind[3)] on transport through quantum dots also elucidates some intriguing physics that may presage devices that exploit the energy associated with single electron charging of small capacitors. These experiments were conducted at cryogenic temperatures and therefore translating such effects into a viable technology faces enormous challenges. Nonetheless, the fact that clear effects from transport of single electrons can be measured opens the door to new areas of research and development. The potential for quantum dots in technology is no longer a question of physics but of fabrication.

At the same time, the fabrication of conventional silicon devices continues to demand greater and greater control of dopant profiles and increased vertical as well as lateral integration. In advanced CMOS the active dimensions of devices are becoming less than quarter-micron. This continued scaling of semiconductor devices poses problems for fabrication while offering enhanced and possibly unique performance. To meet this demand the overall thermal budget (the integrated time-temperature cycles for processing) has become progressively smaller and smaller. A number of powerful new processes have been developed to fabricate semiconductor devices at low temperatures. Molecular-beam epitaxy (MBE), atmospheric-pressure chemical vapor deposition (APCVD), ultra-high vacuum CVD (UHV CVD), and plasma enhanced CVD (PECVD) are key examples. These processes allow band-gap engineering of novel structures in silicon-based heterostructures. Resonant tunneling diodes, heterojunction bipolar transistors, and multi-quantum-well photodetectors are notable examples and are the first of what may become a new phase of silicon solid state electronics that exploits the benefits of scaling and quantum-size effects.

We have observed two-dimensional quantization at an $Si\text{-}SiO_2$ interface where the oxide has been deposited rather than thermally grown. In these devices an accumulation layer is created in the undoped channel just below the interface but relatively close to a doped-substrate electrode. To minimize dopant diffusion and channel doping these devices were fabricated using low-temperature processes. Two series of samples were fabricated using molecular-beam epitaxy (MBE) and ultra-high vacuum chemical vapor deposition (UHV CVD) of silicon followed by plasma-enhanced chemical vapor deposition of SiO_2 The fabrication was particularly demanding since the thin (10-60nm) channel region was deposited directly on a heavily doped Si substrate. Capacitance and electrochemical potential measurements were used to probe the two-dimensional density of states of the electrons in accumulation layers. Our results demonstrate that silicon-based devices can incorporate these new materials and function effectively at low temperatures. Electron mobilities are approximately 4500 $cm^2/V\text{-}s$ at 4.2K for both MBE and UHV CVD samples. These

processes open the door to novel applications and quantum device concepts.

We have also made significant progress in understanding resonant tunneling in silicon-based materials. This is important since resonant tunneling may have technological impact beyond the discrete device and high-frequency oscillator arena. There has been a great deal of work on silicon-based resonant tunneling diodes. Resonant tunneling has been observed in the conduction band as well as the valence band. While the effects in these devices are not nearly as large as in III-V structures, silicon devices can be integrated to a much higher degree. Applications of two-terminal devices are limited at this point, but one cannot completely rule out some novel logic or memory schemes.

We have directly explored the influence of strain on the valence band structure of Si/SiGe quantum wells, using angular-resolved magnetotunneling spectroscopy (ARMS). The in-plane dispersion relations of the resonant levels are probed by a magnetic field applied parallel to the interfaces. This method is unique, in that it measures the local band structure in k-space, in contrast to optical spectroscopy, which averages over all k-space. We detect large non-parabolicity and negative in-plane effective mass for some of the levels. By rotating the magnetic field the energy surface at constant $k_{||}$ is measured, wherewith we see a large anisotropy of the energy levels, with the symmetry axes of light holes and heavy holes being rotated 45° with respect to each other. The valence band structure is less anisotropic in samples with unstrained SiGe quantum wells.

The fact that one can probe the details of SiGe bond structure is evidence of the level of control now possible in silicon-based heterojunctions and quantum-well structures. The additional ability to passivate structures with an stable oxide and form complex three-dimensional structures should provide unique leverage over III-V materials. In short, there are many challenges and opportunities ahead for nanoelectronics. However, the requirements are stringent and the prognosis is not clear. Research in this area must continue to address both fundamental as well as practical issues.

References

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