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AC Characteristics of Super Self-Aligned Si HBTs with SiC_x Emitter

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The report discusses wide-bandgap emitter Si HBTs using Super Self-aligned process Technology (SST) with amorphous silicon carbide (SiCx) emitters. These Si HBTs have a cutoff frequency of 24.0 GHz, the highest ever achieved in wide bandgap emitter Si HBTs. They show smaller emitter-junction capacitance than homojunction transistors. The cutoff-frequency degradation is discussed in relation to emitter resistance and base-collector capacitance. It is shown that emitter resistance is the main factor causing cutoff-frequency degradation.

1. INTRODUCTION

Future high-speed silicon bipolar transistors will use ultra-shallow and highimpurity-concentration bases to obtain short base transit time, low base resistance and high collector-to-emitter break down voltage. A silicon hetero-structure transistor (Si HBT) must be used because emitter-base homojunction cannot provide sufficient current gain in high-concentration-base transistors. However, so far small-size widebandgap-emitter Si HBTs have not been thoroughly investigated for high-speed devices. Thus, special attention should be given to the speed advantages and disadvantages of small-size wide-bandgapemitter Si HBTs.

In this paper, small-size Si HBTs fabricated using Super Self-aligned process Technology $(SST)^{1}$ with amorphous silicon carbide $(SiCx)^{2}$ emitters are reported, and the necessary conditions for high-speed Si HBTs are discussed. It is shown that emitter resistance is the main factor causing cutoff frequency degradation.

2. DEVICE STRUCTURE

Figure 1 shows a cross section of the fabricated Si HBT made using the SST process. Modifications were then made as follows: (1)As the advantages of Si HBTs are clear only in high-speed and shallow-base transistors³), the base region was formed by a boron diffusion process with a base junction depth of about 60 nm and surface concentration of 1 x $10^{19}\ {\rm cm}^{-3}.$

(2)To obtain high collector current, the collector area was fabricated with a low resistivity epitaxial layer of 0.24Ω cm and Selectively Ion-implanted Collector (SIC)⁴).

(3)To ensure good SiCx and metal coverage over the emitter hole surrounded by base polysilicon electrodes, the side walls of the emitter hole were tapered.

(4)To limit emitter resistance, the emitter layer thickness was reduced. The emitter consisted of a 10-nm SiCx layer and a 100-nm polysilicon layer.



Fig. 1. Cross-sectional view of fabricated Si HBT.

3. DEVICE CHARACTERISTICS

Figure 2 shows the h_{FE} versus collector current I_C characteristics of 6 parallelconnected typical Si HBTs (emitter area 0.4x13 μ m²/Tr). The Si HBTs have a peak current gain of 160.

Figure 3 shows f_T-I_C curves of the same devices at collector-emitter voltages (VCE) of 1V, 2V, 3V and 4V. Due to a large dc emitter voltage drop, the f_T at low V_{CE} dropped abruptly at high collector current (I_C). The f_T at high V_{CE} increased in the high current range, and f_{Tmax} at V_{CE} =4V was 24.0 GHz.

Table I shows device parameters for the Si HBTS and control transistors with different SIC implantation doses. The control transistors have phosphorus-doped polysilicon emitters, i.e., homojunction emitters. The SIC dose controlled collector concentration and base width. Therefore, collector current for f_{Tmax} and transit time were changed. The SiCx emitter layers were deposited with two carbon concentrations of about $1 \times 10^{20} \text{cm}^{-3}$ and $4 \times 10^{20} \text{ cm}^{-3}$. As carbon concentration increases, the SiCx layer resistivity and emitter resistance increase. For these test devices, base resistance (R_B), emitter resistance (R_E) and f_T were measured at I_{C} =10 mA/Tr and V_{CE} =3V using an HP network analyzer, and collector junction capacitance (C_{iC}) and emitter junction capacitance (C_{iE}) were obtained by C-V measurement. As the Si HBTs have smaller emitter carrier density, they exhibit smaller C_{jE} than the control transistors. The control transistors have almost the same base width as the Si HBTs because their phosphorus diffusion from the emitter polysilicon electrode is very small during 800°C heat treatment. The current gain of the control transistors is $50 \sim 60$ and is the lower limit to operate logic near circuits. However, the Si HBTs have emitter resistance of about ten times larger. The reason is that N⁺ polysilicon resistivity of the Si HBTs was $5 \times 10^{-2} \Omega$ cm, which was two orders higher due to low deposition temperature (390°C).

4. DISCUSSION

As can be seen in Table I, the Si HBTs have smaller f_T values than the control transistors. This is mainly due to larger emitter resistance of the Si HBTs. The emitter resistance effect on cutoff frequency explained by small-signal analysis. is Figure 4 shows the small-signal equivalent circuit of a bipolar transistor. When emitter resistance exists, the ac potential drop in the emitter resistance must be added to ac



Fig. 2. $h_{FE} = I_C$ curve of 6 parallel-connected Si HBTs with $13-\mu$ m-length emitters.



Fig. 3. f_T-I_C curves for 6 parallel-connected Si HBTs with $13-\mu$ m-length emitters.

Emitter Material	SiCx					
	low carbon concentration		high carbon concentration		Poly Si	
SIC Implantation	low dose	high dose	low dose	high dose	low dose	high dose
ft (GHz)	23.1	22.2	20.3	20.9	26.2	28.9
R E (Ω)	32	51	53	62	6.0	5.8
R B (Ω)	95	100	95	100	120	123
CjC (fF)	27	30	27	30	27	30
CjE (fF)	27				46	

Table I. Device parameters of Si HBTs and control transistors. The values of f_T, emitter resistance and base resistance were measured at V_{CE} =3V and $I_C = 10 \text{mA/Tr}$ using an HP network analyzer.

base-collector voltage for keeping ac collector current (i_C) at a constant value. This additional voltage increases the element (i_1) of the ac base current flowing through the base-collector capacitance (C_{BC}) . Thus the common-emitter short-circuit current gain (h_{21}) decreases, then f_T degrades. From the analysis above, an approximate formula

 $1/2\pi f_{T} = 1/2\pi f_{T0} + R_{E}C_{BC}$

was obtained⁵⁾. In this formula, f_{TO} is the cutoff frequency of the transistor without emitter resistance, and C_{BC} is the base-collector capacitance.

The $f_T - R_E$ relations are shown in Fig. 5. The measured results in Table I are plotted by circles for Si HBTs and by triangles for the control transistors. The calculated curves using the formula are drawn by solid lines for f_{TO} =28.0GHz and C_{BC} =30fF, or 25.6GHz and 27fF. The values of f_{TO} and C_{BC} depend on SIC implantation dose. C_{jC} at V_{BC} =0V was used as C_{BC} . It is shown that the calculated curves well expressed the f_T-R_E relation for both transistors. It is thus concluded that \mathbf{f}_{T} degradation in Si HBTs was caused mainly by emitter resistance.

5. CONCLUSION

Si HBTs using SST with SiCx emitters were fabricated. The obtained maximum cutoff frequency was 24.0 GHz. This is the highest reported value ever achieved in widegapemitter Si HBTs. The emitter-base capacitance was smaller than that of control homotransistors. This is one great advantage of shallow-junction-base transistors over homo-transistors. However, homotransistors have higher cutoff frequency than Si HBTs due the smaller emitter resistance. Tf to widegap-emitter Si HBTs are to surpass Si homotransistors in speed performance, a lower-resistivity emitter material than that in prevailing devices must be developed.

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Fig. 4. Network for defining f_T using small signal equivalent circuit of a bipolar transistor.



Fig. 5. Relation between f_T and emitter resistance. Circles are for Si HBTs, and triangles are for control transistors. Solid symbols are for high SIC dose transistors, and open symbols are for low SIC dose transistors.

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