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A 0.3 μm BiCMOS Technology with Highly Self-Aligned Structures for Deep Submicron ULSIs

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A new highly self-aligned BiCMOS technology is proposed for the low supply voltage deep submicron regime. Main features of the device are (1)reduction of parasitic capacitance by a self-aligned contact process, (2)process simplification due to highly merged structure between bipolar and CMOS. 28GHz bipolar devices and 0.3μm CMOS with a source/drain junction capacitance of 3fF are merged on the same chip. 65ps ECL gates and 60ps CMOS inverters at a supply voltage of 3.3V are demonstrated.

1. INTRODUCTION

BiCMOS technology is now changing from simple compromise between bipolar and CMOS to a strategic technology conforming to diversified ASICs and new system architecture such as RISC. Even for bipolar LSIs, BiCMOS technology becomes increasingly indispensable to overcome the memory packing density limit and power consumption problem[1]. However, performance degradation at low supply voltage is recognized as a major limiting factor for the scaled BiCMOS devices. To solve this drawback, new BiCMOS circuits such as BiNMOS and QC-BiCMOS gate have been proposed[2]. In these circuit configurations, parasitic capacitance of CMOS device puts the serious constraint on high-speed/low-power operation of BiCMOS circuits. Moreover, increasing process complexity will be an unavoidable practical issue in the deep submicron BiCMOS regime.

In this paper, a highly self-aligned BiCMOS technology, which realizes a low parasitic capacitance CMOS structure suited for low supply voltage operation without increasing process complexity, is proposed. This technology will leads to a new low-power, high-speed and low-cost BiCMOS-ULSIs for future intelligent information systems.

2. PROPOSED DEVICE FEATURES

For the scaled BiCMOS device, MOS parasitic capacitance such as source/drain junction capacitance becomes a new limiting factor for high speed BiCMOS gate operation rather than in CMOS circuits(Fig.1). This is because source/drain junction capacitance becomes to be larger than bipolar input capacitance, resulting in bipolar switching time degradation.

Main features of BiCMOS device structure proposed here

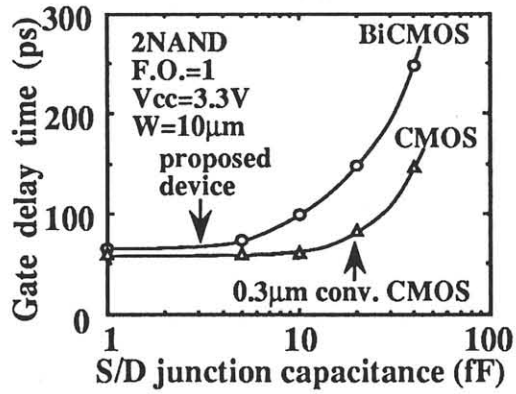

Fig.1 Simulated gate delay time vs source/drain junction capacitance

are as follows(Fig.2), (1)reduction of both CMOS source/drain and bipolar extrinsic base junction capacitances by a self-aligned contact structure, which realizes the junction size less than 0.2μm, resulting in both higher speed and lower power consumption operation. (2)Process simplification due to highly merged device structures in base/source/drain electrode(BSD poly-Si) and emitter/gate electrode(EG W-polycide).

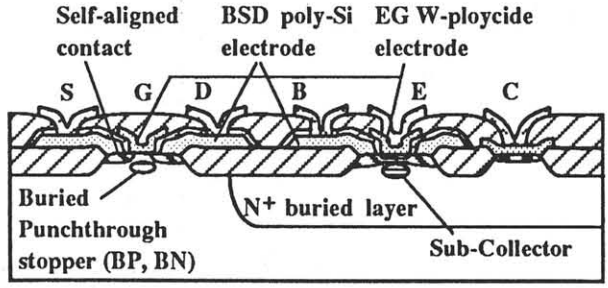

Fig.2 Proposed BiCMOS device structure

3. SELF-ALIGNED PROCESS

The process for the proposed BiCMOS device is based on a double poly-Si self-aligned bipolar technology. Additional some implantation steps are required to merge CMOS devices into the bipolar process. Key technology is a self-aligned contact process(Fig.3) which is mainly consist of (1)definition of both contact region and isolation region by Si_3N_4 spacer, and (2)resist planarization for poly-Si electrode etching. Both CMOS source/drain and bipolar extrinsic base regions are diffused from BSD poly-Si electrodes during its oxidation for the isolation both between emitter and base, between gate and source/drain . Emitter region is also diffused from EG W-polycide electrodes. Total number of masking process including 6 electron direct writing steps was 24 to fabricate by the second level metalization.

Buried punchthrough stopper(BP/BN) under the channel region is one of the unique feature of proposed CMOS structure, which is implanted self-alignedly with source/drain region before gate electrode formation. Lateral struggling of implanted ions strongly influences resulted two dimensional profiles[3], because the mask opening sizes of BSD electrode are comparable or less than the projected range of BP/BN ion implant. Two dimensional Monte Calro simulations for BP/BN layer shows that significant decreases of impurity concentration with shortening channel length(Fig.4).

Implantation conditions are 50keV-boron(Nm(1)) and 140keV-boron(Nm(2)) ions for BP layer, 300keV-arsen(Nm(1)) and 390keV-phosphorous(Nm(2)) ions for BN layer. Appropriate ion doses are 1.5 to 2 times larger than those of the conventional MOS devices to avoid punchthrough phenomena in the short channel devices. Self-aligned sub-collector implant and rapid thermal annealing were also employed for bipolar devices.

Almost expected device structure was obtained(Fig.5).

4. DEVICE PERFORMANCE

CMOS device Well controlled threshold voltage around 0.3V of n-channel and -0.5V of p-channel devices were realized(Fig.6). Drain current are almost the same level as con-

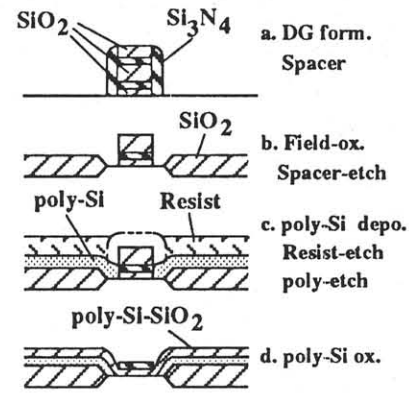

Fig.3 Self-aligned contact process flow

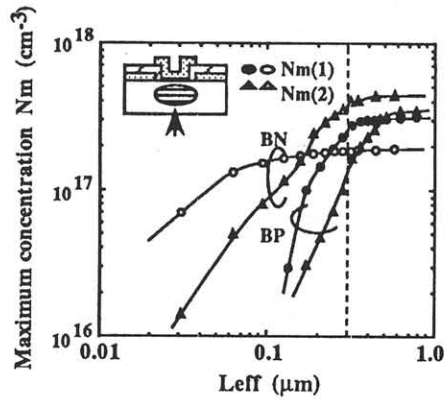

Fig. 4 Monte Calro simulated Leff dependences of Nmax in BP/BN layer

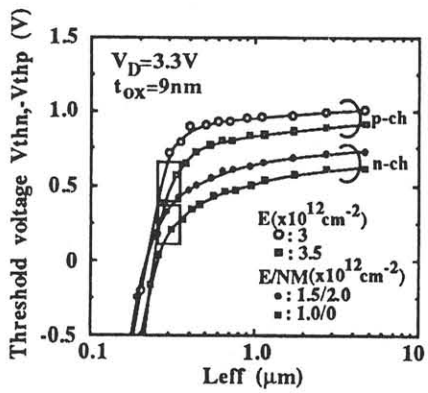

Table 1. CMOS performance

Ids *	n	4.6mA
	p	3.1mA
Vth	n	0.3V
	p	-0.5V
Cjsd	n	0.27fF/μm
	p	0.35fF/μm
Cgov	n	0.12fF/μm
	p	0.17fF/μm
tox		9nm

*Leff=0.3μm
Weff=10μm,Vcc=3.3V

Fig. 6 Vth-Leff relationships

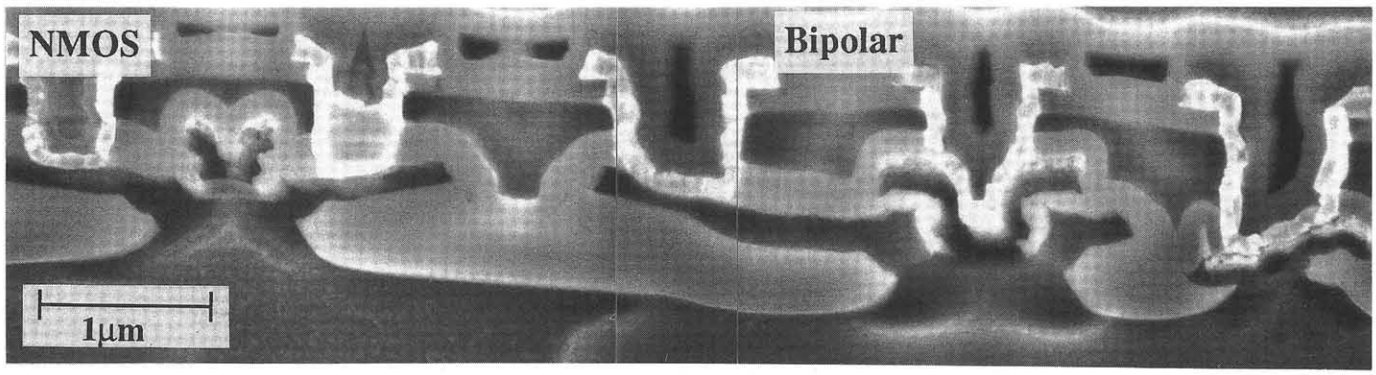

Fig.5 SEM micrographs of the fabricated device

ventional 0.3μm devices(Table 1). Source/drain junction capacitance was reduced down to 0.27-0.35fF/μm by the self-aligned contact structure, which is 20% of conventional 0.3μm CMOS. Overlapping capacitance between gate and source/drain is 0.12-0.17fF/μm, which is one fifth smaller than that of SST-BiCMOS[4].

Bipolar device No generation-recombination leakage current between emitter and base was observed in Gummel plots. Maximum cut-off frequency of was improved up to 28GHz due to mainly sub-collector(SC) which was formed by 100keV phosphorous ion implant with dose of $1x10^{13}$ cm^{-2}(Fig.7). Rapid thermal annealing for emitter activation is also effective to improve performance. Breakdown voltage between emitter and base, emitter and collector of these devices are 4.5V and 4.2V, respectively. By convectional furnace emitter derive with 850°C for 15min, cut-off frequency of 25GHz can be achieved by decreasing implant doses for intrinsic base(IB). Base resistance of 350-400Ω was obtained (Fig.8).

5. BASIC GATE PERFORMANCE

ECL gate delay time of 65ps at switching current of 1mA was obtained, which is 1.5 times faster than our 0.5μm BiCMOS devices(Fig.9). Gate delay time of CMOS inverter is also around 60ps at a supply voltage of 3.3V(Fig.10), which is 1.2 times faster than a conventional 0.3μm CMOS devices with source/drain junction capacitance of 15fF. Overlapping capacitance between gate and source/drain is almost negligibly small in the circuit operation.

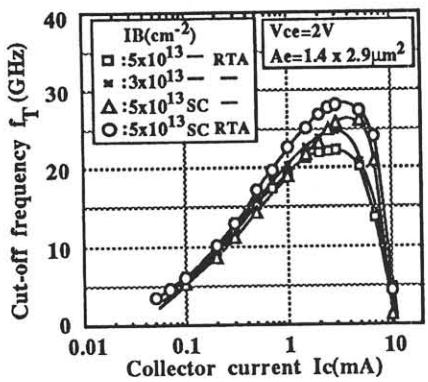

Fig.7 Ic dependences of cut-off frequency

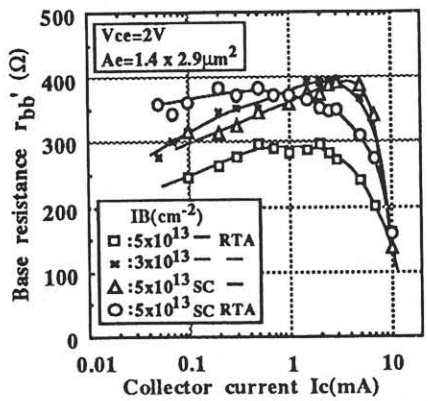

Fig.8 Ic dependences of base resistance

6. CONCLUSION

A novel self-aligned BiCMOS device technology has been proposed. The 28GHz bipolar devices and low parasitic capacitance 0.3μm CMOS have been merged on the same chip without increasing process complexity. This demonstrates that the proposed BiCMOS device will pave the way to high speed ULSIs for the coming low supply voltage era.

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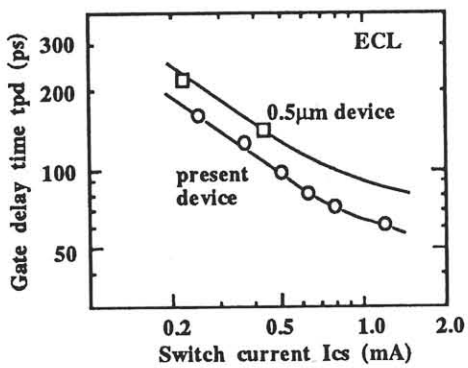

Fig.9 ECL gate performance

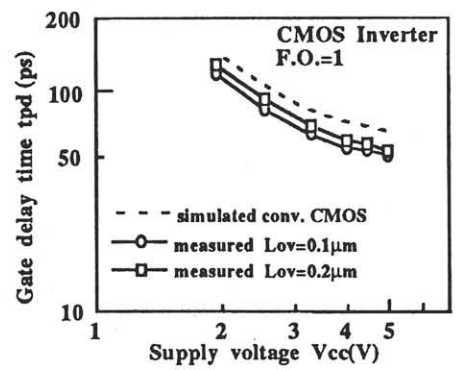

Fig.10 CMOS inverter performance