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Fabrication of Double-Gate Thin-Film SOI MOSFETs Using Wafer Bonding and Polishing

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Double-gate thin-film SOI MOSFETs have been developed for high-speed CMOS-ULSI. The important processes include planarization of the bonded surface by CVD SiO_2 polishing, and low-temperature wafer bonding using BPSG film. The characteristics of the device are dramatically improved by using a double-gate structure with a 50 nm-thick Si layer. The drain current of a double-gate n-MOSFET is 3 times higher than that of a single-gate n-MOSFET. The maximum transconductance is 150 mS/mm, more than twice that of a single-gate n-MOSFET.

1. Introduction

Ultra-thin SOI MOSFETs are expected to be free of kink effects and provide an excellent subthreshold slope and an increased current when the channel region is fully depleted by the gate potential.[1-3]

Recently, SOI MOSFETs having new gate structures have been proposed to achieve better performance. High transconductance and reduced short-channel effects have been demonstrated in such structures as double-gate[4-5], vertical-gate[6] and gate-all-around[7] devices.

This paper describes a newly developed process to fabricate double-gate SOI MOSFETs. The fabrication process consists of SiO_2 polishing and wafer bonding, which provides the double-gate with a very simple structure. In addition, the improved electrical characteristics of the fabricated SOI MOSFETs are described.

2. Double-Gate SOI MOS Structure

Figure 1 shows the double-gate SOI MOSFET structure. The back-gate is buried in the insulator. The thin Si layer has a crystal quality equal to that of bulk Si. This structure is planar and compatible with conventional ULSI designs.

3. Fabrication

Double-gate SOI MOSFETs are fabricated as shown in Figure 2. (a) A 200-nm-thick field oxide is formed by conventional selective oxidation. It acts as a polishing stopper. A 500-nm-thick CVD SiO_2 layer is deposited, and etched by RIE to open the window for the back-gate. (b) The back-gate oxide is formed. The window is filled with polysilicon by LPCVD and then planarized by selective polishing. (c) An 800-nm-thick CVD SiO_2 is deposited and then, smoothed by polishing. (d) The BPSG film is deposited on the base wafer. The Si wafers are bonded by pulse-field-assisted bonding. (e) The Si active

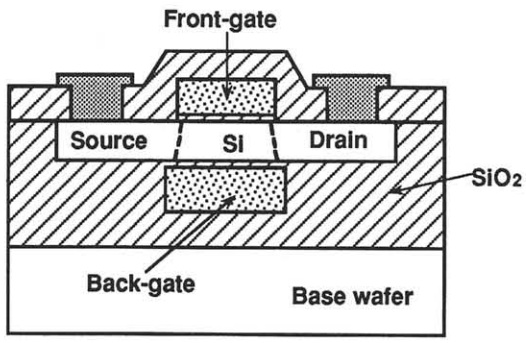

Figure 1 The double-gate SOI MOSFET

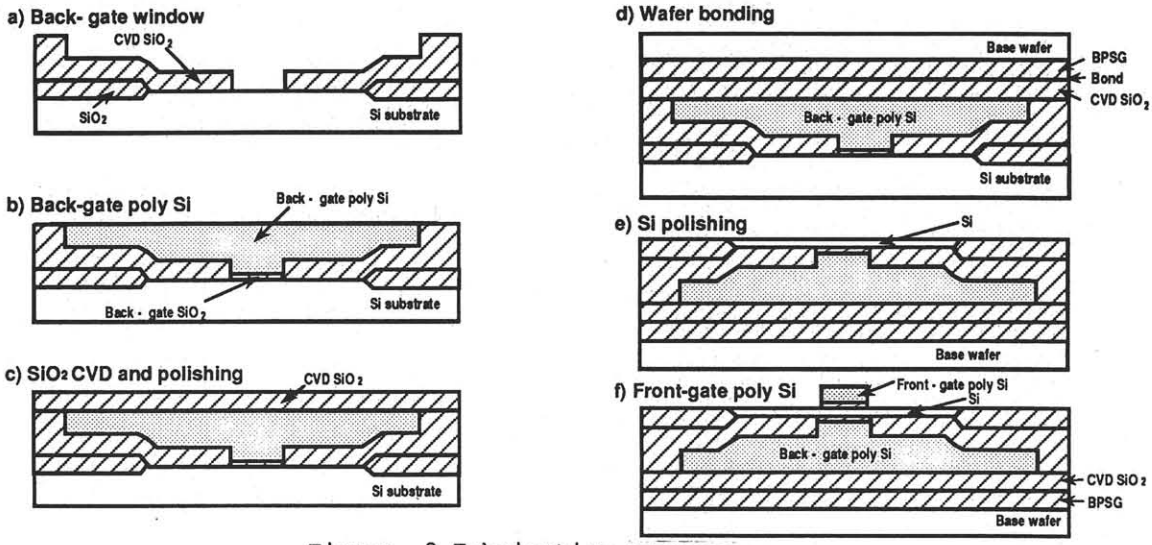

Figure 2 Fabrication process

layer is thinned by selective polishing. The Si active layer thickness is determined by a field-oxide stop layer. (f) The front gate is formed by conventional processing.

4. Key Processes

4,1 Planarization by polishing CVD SiO_2

Figure 3 are SEM micrographs taken before and after planarization of the CVD SiO_2 layer. For SiO_2 polishing, a polyurethane pad and colloidal silica are used. After polishing, the CVD SiO_2 layer is uniformly smooth. Figure 4 shows the flatness of the CVD SiO_2 layer as a function of the polished SiO_2 thickness. The step height linearly decreases, as the polished SiO_2 thickness increases.

4,2 Bond with base wafer

Figure 5 shows the bond strength. The two wafers are bonded using pulse-field-assisted bonding at a 950 °C in a 0.1 Pa N_2 atmosphere. The bond strength of the polished CVD-SiO_2/BPSG film exceeds 2000 kgf/cm^2. This value is comparable with that of conventional-silicon/thermal-oxide bonded wafer, strong enough for LSI fabrication.

5. Electrical characteristics

An SEM micrograph is shown in Figure 6. The SOI thickness is 50 nm. The back- and front-gate oxide are 22-nm-thick. The gate material used p^+

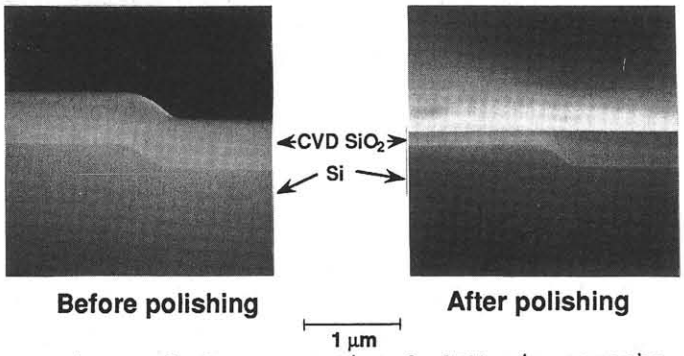

Figure 3 Cross-sectional SEM micrographs showing the planarization of the CVD SiO_2 layer

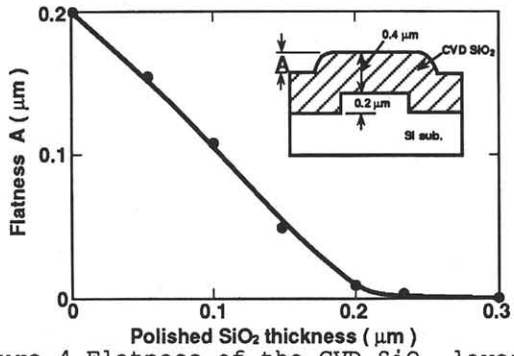

Figure 4 Flatness of the CVD SiO_2 layer as a function of polished SiO_2 thickness

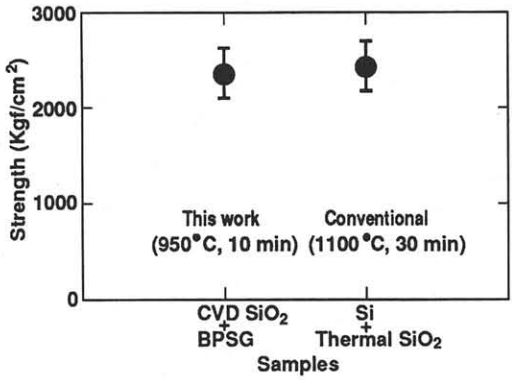

Figure 5 Wafer bond strength

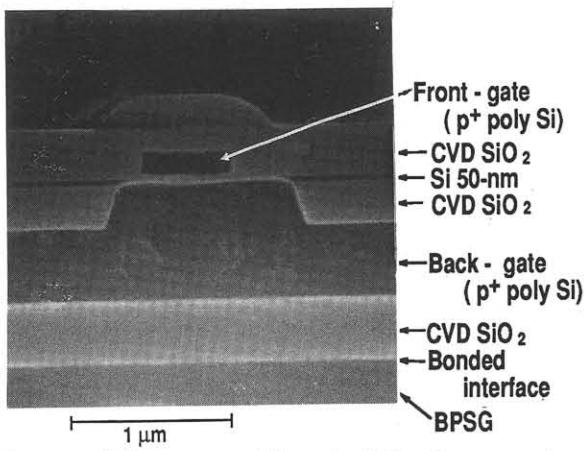

Figure 6 Cross-sectional SEM micrograph of double-gate SOI MOSFET

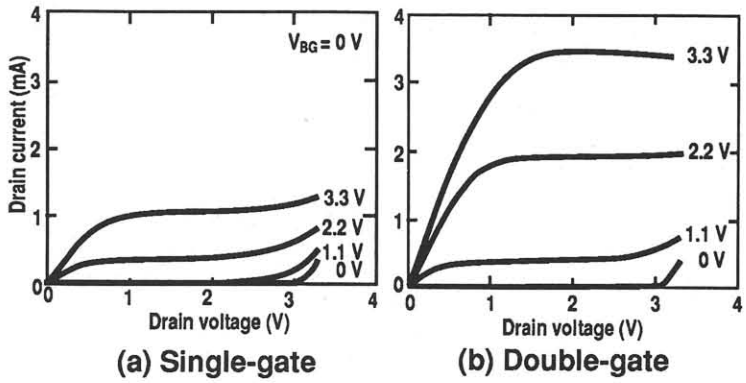

Figure 7 Current-voltage characteristics for (a) single-gate n-MOSFET and (b) double-gate n-MOSFET (L/W = 0.6/10 μm, T_{ox} = 22 nm)

polysilicon for the threshold voltage control.

Figure 7 shows current-voltage characteristics for both double-gate and single-gate n-MOSFETs. The gate length is 0.6 μm and the gate width is 10 μm. The drain current of the double-gate n-MOSFET is 3 times higher than that of single-gate n-MOSFETs. Figure 8 shows the transconductance (g_m) at a drain voltage of 2 V and a gate length of 0.6 μm. The g_m of the double-gate n-MOSFET is 150 mS/mm at gate voltage of 2 V. The g_m increase is remarkably in double-gate operation as compared with single-gate operation, especially at low gate voltages due to the carriers injected from the source to the channel region.

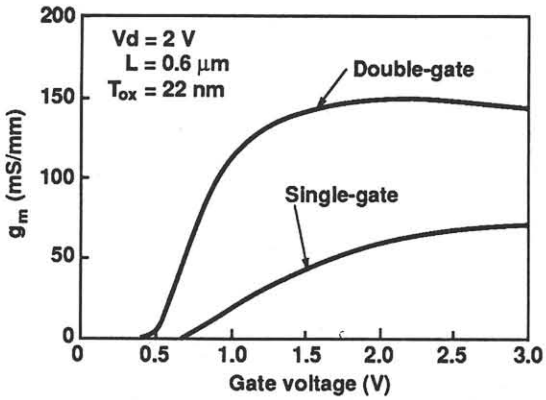

Figure 8 g_m of double- and single-gate n-MOSFETs

6. Summary

Using wafer bonding and polishing processes, we fabricated p^+ polysilicon double-gate n-channel MOSFETs that have a planar layout and are compatible with conventional ULSI designs. We demonstrated the superiority of double-gate operation, having both high drain current and high transconductance. Double-gate SOI MOSFETs having a thin Si active layer provides a promising approach to high-speed ULSI devices.

7. Acknowledgement

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8. References

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