Wafer Bonding and Thinning for High-Speed SOI Epitaxial-Base Transistors

Atsushi FUKURODA, Toru MIYABO, Manabu KOJIMA, Tetsu FUKANO, Naoshi HIGAKI, Tatsuya YAMAZAKI, Toshihiro SUGII, Yoshihiro ARIMOTO, and Takashi ITO

Fujitsu Laboratories Ltd.
10-1 Morinosato-Wakamiya, Atsugi 243-01, Japan

A 1-μm-thick silicon-on-insulator (SOI) with an implanted buried layer is fabricated by wafer bonding and selective polishing. Photoepitaxial base transistors (EBTs) fabricated on the SOI have a cutoff frequency of 32 GHz without using an epitaxial collector.

1. Introduction

The SOI bipolar transistor has demonstrated high speed and tolerance to radioactivity. Using a photoepitaxial base, we obtained a very thin, highly doped base layer for high-speed bipolar transistors. This paper reports a technique for fabricating an SOI with an implanted buried layer for high-speed EBTs. It also discusses the features of SOI EBTs. Surface roughness increases at highly implanted wafers and prevents them from bonding uniformly. This paper explains how to obtain tight, voidless bonding and uniform SOI film thinning.

2. SOI Fabrication

The fabrication process is shown in Fig. 1. We used n-type wafers for devices, thermally oxidized 4-inch-diameter Si (100) wafers for base wafers. The SiO₂ on the base wafers is 1 μm thick. To make a thin n⁺ buried layer, we implanted 5x10¹⁵ cm⁻² doses of 25 keV As⁺ into the n-type wafer through a thin oxide layer. The thin oxide was removed by HF before bonding. This enables us to obtain a thin buried layer and an active collector layer without epitaxy.
Bonded SOI wafers were made by pulse-field-assisted bonding to overcome surface roughness at 800°C in a 0.1 Pa N₂ atmosphere. Bonded wafers were annealed at 1000°C for 30 minutes in a N₂ atmosphere to reinforce the bond. No voids were observed. Surface grinding and polishing enabled us to thin the SOI to 3–5 μm with a variation of 0.6 μm.

To lower variations in the SOI film, we selectively polished the SOI by using a SiO₂ polishing stopper. First, the SOI layer was etched by KOH retaining Si islands 0.8 by 0.8 mm. Next, polishing stoppers 1 μm thick and 180 μm wide were made by CVD SiO₂ in the gaps between islands. In selective polishing, a polyurethane pad and a thinned colloidal silica with amine were used. The polishing rate for Si is over an order of magnitude larger than that for SiO₂. The most suitable work revolution for selective polishing was prepared to avoid dents in the center of the Si island (Fig. 2). We found that this was best attained with a high work revolution. After selective polishing of SOI film to 1 μm thick at 150 rpm, the thickness variation of the SOI in a typical wafer became less than 0.1 μm (Fig. 3).

3. Device Features

Transistor regions (Fig. 4) were completely isolated by LOCOS. The n’ buried layer is 0.7 μm thick and active collector layer 0.3 μm thick. The sheet resistance of the buried layer is about 20 Ω/sq.

A base region was grown at 600°C using photoenhanced low-temperature epitaxy and simultaneously doped by B to $6 \times 10^{18}$ cm⁻³. The epitaxial base is less than 0.1 μm thick.

The emitter of the EBTs fabricated on the SOI (Fig. 5) is 0.5 by 5.0 μm. Typical I-V characteristics of the SOI-EBT are given in Fig. 6. The C-E, C-B, and E-B breakdown voltage are 5.0, 11.5, and 3.5 V. The collector-to-collector breakdown voltage exceed 200 V, indicating complete isolation. The high cutoff frequency of 32 GHz was obtained. It will be further improved by reducing the epitaxial base thickness.
4. Conclusion

We made a fully isolated SOI with an n* buried layer using wafer bonding and selective polishing. We fabricated EBTs on the SOI and obtained the high cutoff frequency of 32 GHz. This SOI technique is very promising for high-speed devices.

5. References

5) Y. Arimoto et al., 46th Device Research Conf., 1A-6 (1988).