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# A Novel Fabrication Technique of Multi-Layer-Stacked SOI Structures Applicable to 3D-ICs

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In this study, in order to investigate the feasibility of three-dimensional ICs fabricated using the combined techniques of Lateral-Solid Phase Epitaxy (L-SPE) and Selective Epitaxial Growth (SEG) of Si, we fabricated a 5-layer-stacked SOI structure and studied its characteristics. In this procedure, both epitaxy of Si for SEG on seeded windows and deposition of amorphous-Si for L-SPE were performed using ultra low pressure chemical vapor deposition. As results, an equal single crystalline SOI region was successfully obtained on each layer. We also fabricated n-MOS FETs onto a top layer. A maximum $\mu_{FE}$ of 617 $cm^2/V \cdot sec$ was obtained. This is the first report on the single crystalline 5-layer-stacked SOI structure.

## INTRODUCTION

Lateral-Solid Phase Epitaxy (L-SPE) is one of the most promising techniques for fabricating Silicon-on-Insulator (SOI) structures suitable for Three-Dimensional ICs (3D-ICs) and high-speed, high-density ICs. However, in order to realize SOI-devices implementation using L-SPE, additional methods for expanding of L-SPE length are needed. Further, to realize the practical application of 3D-ICs, L-SPE length and crystalline quality equivalent to single SOI layers must be achieved for each layer.

We propose a new fabrication technique for a multi-layer-stacked SOI structure. In this procedure, deposition of amorphous-Si (a-Si) for L-SPE is performed by Ultra Low Pressure Chemical Vapor Deposition (U-LPCVD) utilizing the pyrolysis of $Si_2H_6$. L-SPE is accomplished by furnace annealing at about 600°C in an ambient of $N_2$. In addition, filling of seeded windows is accomplished by Selective Epitaxial Growth (SEG) of Si. An a-Si film deposited as described above has a superior film-quality. Thus, using it promotes the expansion of L-SPE length on each layer. Thus, this procedure offers the advantage of being a low-temperature process, expanding of SOI area on each layer and of simplifying planarization processes(1),(2).

In this paper, we will discuss the L-SPE characteristics of non-doped a-Si films deposited as described above and SEG characteristics of Si grown using U-LPCVD utilizing the pyrolysis of $SiH_4/H_2$. We will also discuss the L-SPE characteristics and TEM observation of a 5-layer-stacked SOI structure fabricated using the combined techniques of L-SPE and SEG. Furthermore, we will discuss the electrical characteristics of n-MOS FETs fabricated on the 5th-layer.

## EXPERIMENTAL

A schematic diagram of the apparatus for the U-LPCVD used in this study is shown in Figure 1. The reaction chamber and the preparation chamber are loadlocked by a gate valve. The base pressure of each chamber is kept at about 5 x $10^{-8}$ Torr.

P-type 5-7 Ω-cm (100) Si wafers covered with $SiO_2$ striped patterns oriented to the <100> direction were used as a substrate. Prior to SEG or deposition of a-Si, the substrate was cleaned using an RCA process. The substrate was then exposed in an ultraviolet/ozone cleaning system for 2 minutes to reduce surface carbon contamination. A thin oxide layer formed during exposure was removed by dipping into diluted HF. After being dipped into deionized water for a few seconds, the substrate was spin-dried. Immediately after cleaning, the substrate was placed into the preparation chamber, and the chamber was pumped out to 1 x $10^{-8}$ Torr.

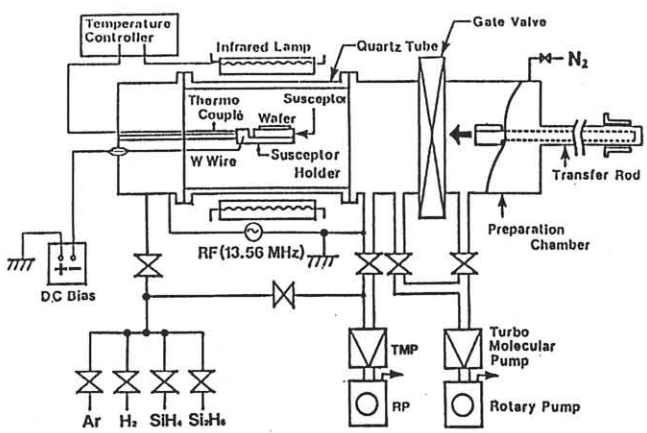


Figure 1 Schematic diagram of the apparatus for the U-LPCVD

The deposition of an a-Si film was performed at 490°C, the deposition rate of which was 500 Å/min. SEG, on the other hand, was performed at 890°C, with a growth rate of 90 Å/min. L-SPE was accomplished by furnace annealing at 590°C in an ambient of $N_2$.

For the fabrication of 5-layer-stacked structures, the thickness of $SiO_2$ films for electrical isolation between each SOI layer was 5,000 Å, and all deposited a-Si films for fabrication of each SOI layer were 5,000 Å. L-SPE was accomplished by furnace annealing for 24 hours. After formation of each stacked SOI layer using L-SPE, defects incorporated into each layer were removed by furnace annealing at 1050°C for 1 hour in an ambient of $N_2$.

N-MOS FETs were fabricated onto the island, as well as active SOI layer using a conventional poly-Si gate n-MOS process.

## RESULTS AND DISCUSSION

Figure 2 shows an annealing time dependence for L-SPE length for an a-Si film on a thin $SiO_2$ layer. The maximum L-SPE length of 14 μm was obtained for the non-doped a-Si film with a thickness of 1.5 μm. This is the highest L-SPE length for a non-doped a-Si film reported to date[3]. From this result, it is assumed that an ultra-low background pressure and high-rate, low-temperature deposition reduce the formation of micro-crystals and prevent residual impurities from entering the a-Si films, the reduction of which create a prolonged elapse in random nucleation generation and enhance the growth speed of L-SPE, respectively.

Figure 3 shows a cross-sectional TEM view of a SEG layer. It is clear that the seeded windows have been completely filled. No poly-crystalline nuclei are observed on the $SiO_2$ layers. Few defects are observed in the SEG layer. These results indicate that this SEG technique is suitable for the filling of seeded windows.

Figure 4 shows the cross-sectional TEM view of a 5-layer-stacked SOI structure fabricated using SPE and SEG. As can be seen from this figure, each stacked layer of 5,000 Å thickness is a single crystal, although high-density dislocation defects are still observed in each L-SPE region.

Figure 5 shows the annealing time dependence of L-SPE length for each layer, in which all maximum L-SPE length are equal at about 8 μm. These results indicate that an equal SOI area can be obtained for each layer using this procedure.

Figure 6 shows the cross-sectional Scanning Ion Micrograph (SIM) view of an n-MOS FET fabricated onto a top layer. In this case, a source region is located on the filling of the seeded windows, and the channel region is fully covered by the L-SPE area.

Figure 7 shows the typical $I_D$-$V_G$ characteristics of an n-MOS FET on a top layer. Threshold voltage, $V_{TH}$, is 0.4 V. A subthreshold swing, S, of 95 mV/dec at $V_{sub}$ = 0 V and leakage current, $I_{DS}$, of 0.07 pA/μm were obtained.

Figure 8 shows the dependence of field effect mobility, $\mu_{FE}$, on gate distance, (X), away from the edge of a seeded window, compared with those of n-MOS FETs fabricated onto a single L-SPE layer on a thin $SiO_2$ film. From X = 0 to 4 μm, $\mu_{FE}$ values of higher than 500 $cm^2/V \cdot sec$ were obtained for each layer. These results indicate that equal crystalline quality can be obtained for each layer, and also agree with the estimates obtained from the results, as shown in Figure 5. The maximum $\mu_{FE}$ is 617 $cm^2/V \cdot sec$ for the n-MOS FET of X = 2 μm. These data are comparable to those of bulk n-MOS FETs.

## CONCLUSION

The results obtained from this study indicate that each layer of the multi-layer-stacked SOI structure can have an equal L-SPE area and crystalline quality. We conclude that the realization of 3D-ICs using the combined techniques of L-SPE and SEG is feasible, although investigation of RTA procedures to recover high-density defects in the SOI layers is still needed.


## ACKNOWLEDGEMENT

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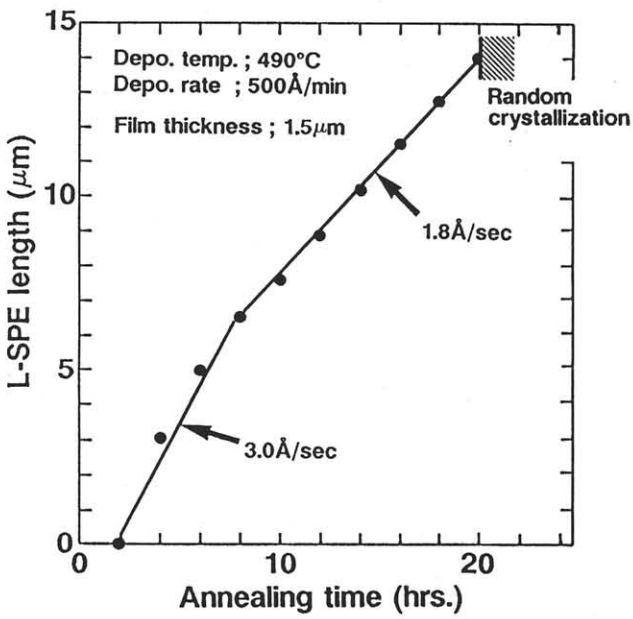


Figure 2 Annealing time dependence for L-SPE length for an a-Si film on a thin $SiO_2$ layer

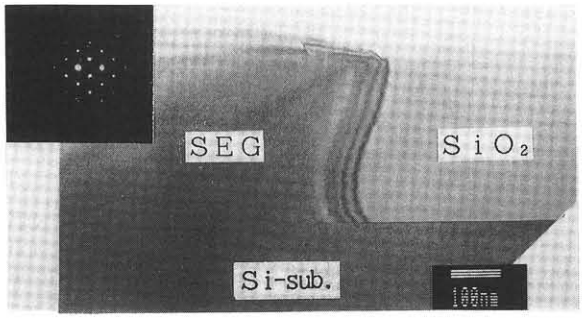


Figure 3 Cross-sectional TEM view of an SEG layer

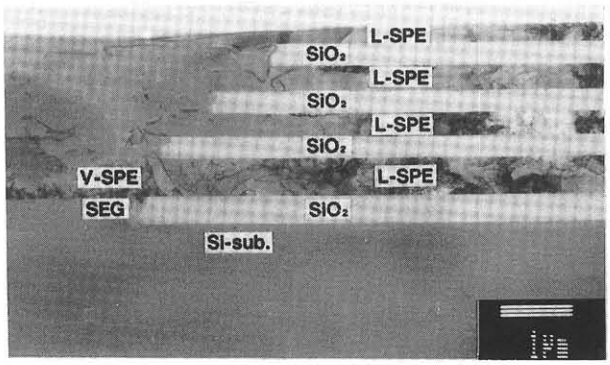


Figure 4 Cross-sectional TEM view of a 5-layer-stacked structure

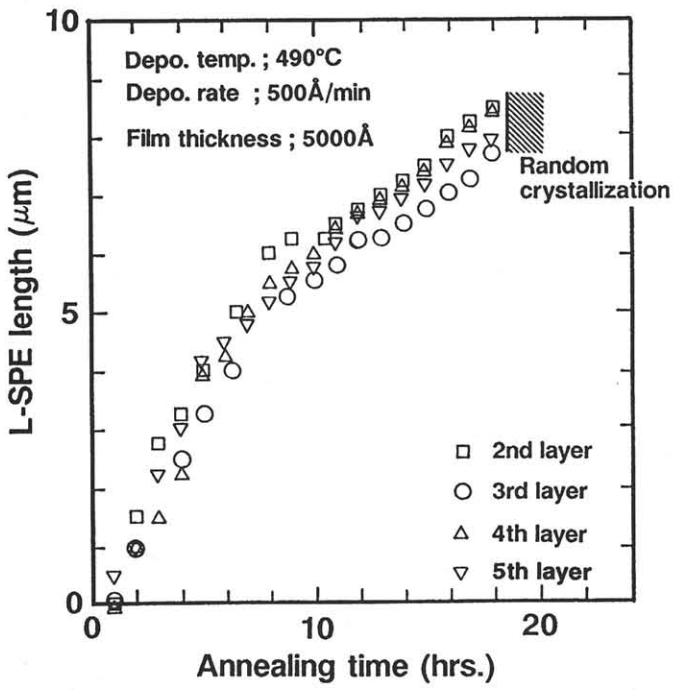


Figure 5 Annealing time dependence of L-SPE length for each layer

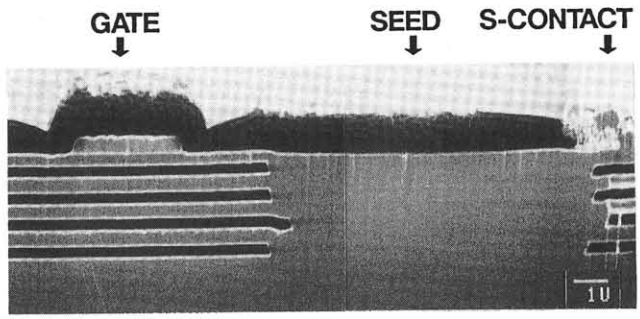


Figure 6 Cross-sectional SIM view of an n-MOS FET fabricated onto a top layer

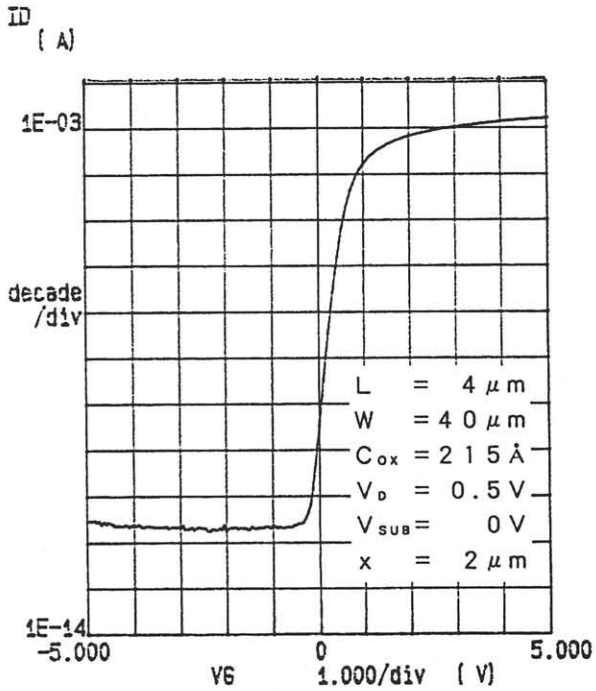


Figure 7 Typical $I_D$-$V_G$ characteristics for an n-MOS FET fabricated on a top layer

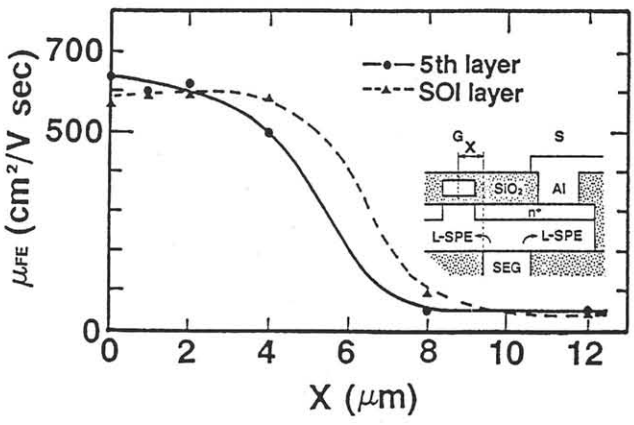


Figure 8 Dependence of $\mu_{FE}$ on gate distance, (X), away from the edge of an seeded window