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Leakage Current Reduction in Sub-Micron Channel Poly-Si TFTs

H. Kitajima, Y. Suzuki and S. Saito

Microelectronics Research Laboratories, NEC Corporation
1120, Shimokuzawa, Sagamihara 229, Japan

The fabrication process to shorten the channel length of poly-silicon PMOS TFT with keeping low leakage current has been investigated. The oxidation after BPSG deposition under the lower source/drain implantation, which can reduce the required offset length, is effective to reduce the leakage current, and to eliminate the gate-to-drain offset. F^+ implantation is more effective to increase the I_{on} of TFTs by subthreshold swing improvement. This process was also effective to shorten the channel length. As the result, I_{on} of $-5x10^{-9}$ A/μm and I_{off} of $-1x10^{-13}$ A/μm were obtained at Vd=-3V for non-offset TFT with 0.8 μm gate length.

1. Introduction

Recently, poly-Si PMOS TFTs (Thin Film Transistors) have been studied to improve SRAMs[1-2]. Leakage current reduction in shorter channel length poly-Si TFTs is a key in order to realize low stand-by power in mega bit SRAMs. The gate-to-drain offset structure has been proposed to minimize the leakage currents. However, this structure is not suitable in future SRAMs because of enlargement in size. This paper reports on the control of charge state to reduce the leakage current in sub-micron channel length poly-Si TFTs without using offset structures. Source/drain implantation conditions, oxidation effect and F^+ implantation effect are mainly investigated.

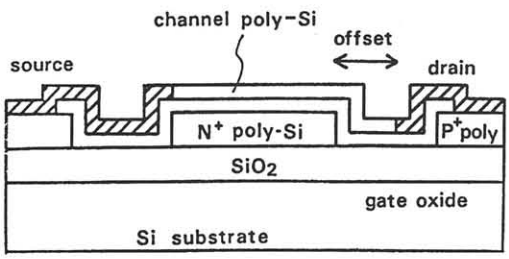

Fig.1 Cross-sectional view of poly-silicon PMOS TFT.

2. Device fabrication

Figure 1 shows a cross-sectional view of the poly-Si TFT with the gate-to-drain offset structure. This structure was fabricated as follows. A 45nm thick gate SiO_2 layer was deposited on N^+ poly-Si gate electrodes by LPCVD method. A 40nm thick amorphous silicon layer was deposited at 550°C using Si_2H_6, and then crystallized at 600°C for 6 hours in N_2. Phosphorus ions were implanted in the poly-Si film at a dose of $5x10^{12}cm^{-2}$. Source and drain regions were formed by 50keV BF_2 implantation with photoresist mask. After removing the photoresist, fluorine ions with 20keV were implanted through 50nm thick $SiO2_2$ at a dose of $3x10^{15}cm^{-2}$. A 400nm thick BPSG layer was deposited, and annealed at 850°C for 30 minutes in N_2 or H_2-O_2. Finally, H_2 anneal was done at 400°C.

3. Results and discussions

The BF_2 dose for source and drain regions is investigated to minimize the offset length. Figure 2 shows Id vs. Vg characteristics for offset length of 0 and 0.3μm. By decreasing the BF_2 dose from $1x10^{15}$ to $1x10^{14}cm^{-2}$, the offset length required to minimize the leakage currents can be reduced by 0.1-0.2μm. I_{on} of TFTs with 0.3μm offset length are reduced by the series resistance of the offset regions.

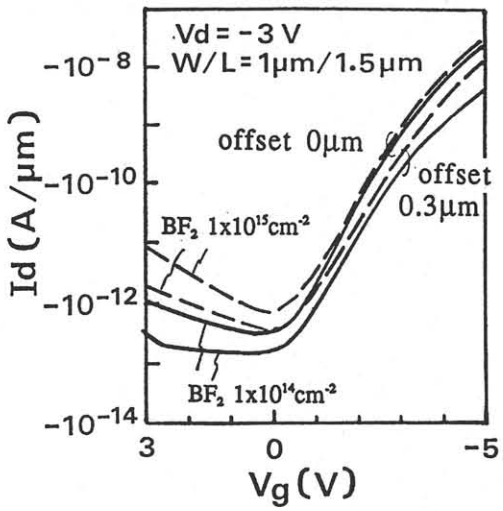

Fig.2 Id-Vg characteristics of poly-silicon TFT for offset length of 0 and 0.3μm. The annealing condition was 850°C for 30 minutes in N_2.

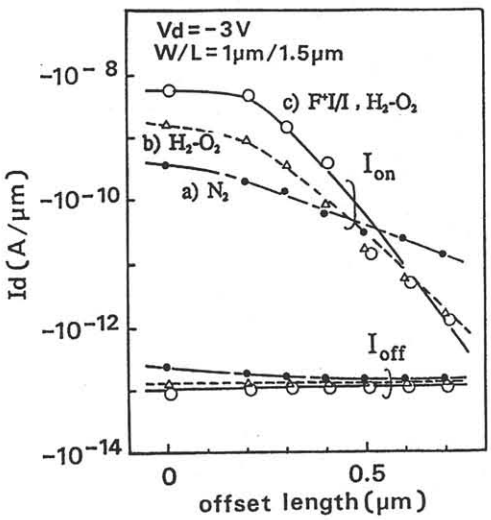

Fig.3 I_{on} and I_{off} vs. offset length for three treatments. a)850°C in N_2 for 30 minutes, b)850°C in H_2-O_2 for 10 minutes after in N_2 for 20 minutes and c)F^+ implantation and treatment b).

In order to improve the TFT characteristics, oxidation after BPSG layer deposition and F^+ implantation were attempted. Figure 3 shows I_{on} and I_{off} vs. offset length relation under BF_2 dose of $1x10^{14}cm^{-2}$ for three treatments; a)850°C annealing in N_2 for 30 minutes, b)850°C annealing in H_2-O_2 for 10 minutes after in N_2 for 20 minutes and c)F^+ implantation and treatment b). Non-offset TFTs' I_{off} was defined as the minimum leakage current, and offset TFTs' I_{off} was measured at the same gate voltage as non-offset TFTs. I_{on} was measured at the gate voltage of -3V increase from the I_{off} gate voltage. I_{on} increase by 5 times and I_{off} decrease were obtained by the oxidation for non-offset TFTs. The channel poly-Si film is oxidized even after thick BPSG layer deposition, and the TFT characteristics may be improved by rapid oxidation along grain boundaries.

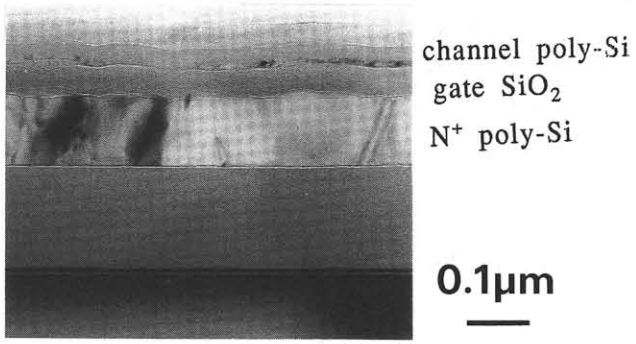

Fig.4 Cross-sectional TEM micrograph of channel poly-Si afetr F^+ implantation.

F^+ implantation before BPSG deposition was more effective to increase I_{on} by subthreshold swing improvement. Figure 4 is the cross-sectional TEM micrograph of channel poly-Si region just after F^+ implantation. Topside channel poly-Si became amorphous by F^+ implantation. It may be important for TFT characteristics improvement that the channel poly-Si at the Si/SiO_2 interface remained poly-crystalline. Number of dangling bonds in the poly-Si films was measured by ESR (Electron Spin Resonance) method. For ECR measurement, amorphous silicon deposited on quartz substrates was crystallized at 600°C for 6 hours in N_2, annealed at 850°C after F^+ implantation, and then annealed in H_2 at 400°C. Number of dangling bonds, measured of about $1x10^{18}cm^{-3}$, was slightly reduced by F^+ implantation. Therefore, the improvement of TFT characteristics with F^+ implantation should be the passivation effect by fluorine atoms mainly at the Si/SiO_2 interface.

Figure 5 shows I_{off} vs. drain voltage for non-offset TFTs. The oxidation and F^+ implantation are effective for passivation of the defect in the poly-Si films. The oxidation after BPSG deposition can reduce the leakage current not only at low electric field (G-R induced) but at high electric field, while F^+ implantation reduce the leakage current at low electric field.

The offset length can be reduced by the combination of F^+ implantation and the oxidation as shown in Fig.3. Therefore, these processes are expected to reduce the channel

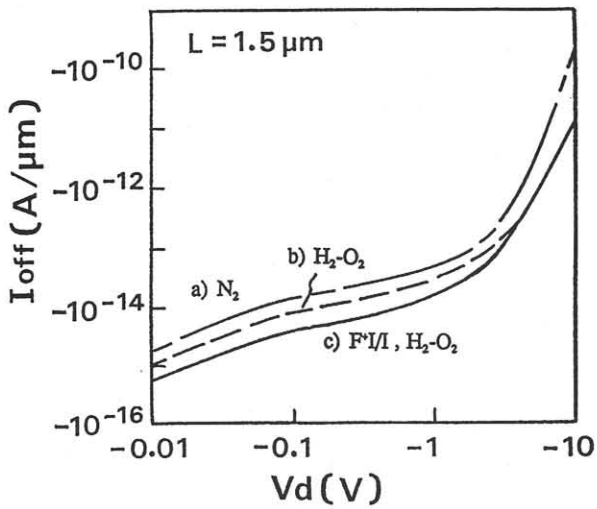

Fig.5 I_{off} -Vd characteristics of non-offset TFTs for treatment a)-c).

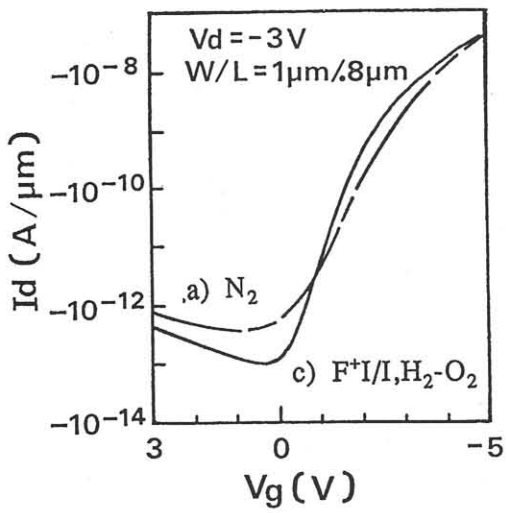

Fig.6 Id-Vg characteristics of non-offset TFTs for treatments a) and c).

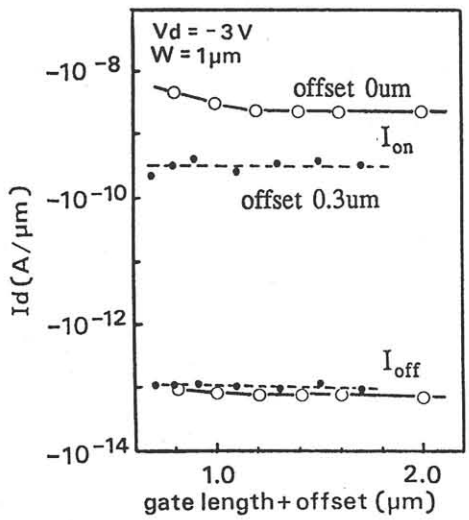

Fig.7 I_{on} and I_{off} vs. gate length plus offset length for treatment c).

length of TFT without increasing the leakage current. From Id-Vg characteristics of non-offset TFTs in Fig.6, it is shown that the F^+ implantation and subsequent oxidation can improve I_{on}/I_{off} ratio by one order or more at Vd=-3V for 0.8 μm gate length without offset structures. Figure 7 shows I_{on} and I_{off} dependence on gate length plus offset length in the optimized conditions. Under the limited TFT size along the channel direction, larger current can be obtained in the case of non-offset structure than the case that the channel length is divided into the gate length and the offset. As the gate length decreases from 2.0 to 0.8μm, I_{on} increases with keeping low leakage current.

4. Summary

The fabrication process to shorten the channel length of poly-silicon PMOS TFT with keeping low leakage current has been investigated. The oxidation after BPSG deposition under the lower source/drain implantation is effective to reduce the leakage current, and to eliminate the offset. In combination with F^+ implantation, which is more effective to increase the I_{on} of TFTs, lower I_{off} and subthreshold swing improvement were accomplished. I_{on} of -5×10^{-9} A/μm and I_{off} of -1×10^{-13} A/μm were obtained at Vd=-3V for non-offset TFT with 0.8 μm gate length.

Acknowlegment

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References

1) M.Ando et al., 1988 Symp. VLSI CIR Dig. (1988) 49
2) S.Ikeda et al.,IEDM Tech. Dig. (1990) 469