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Reviews and Prospects of Deep Sub-Micron DRAM Technology

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The state of the art in DRAM technology is reviewed, emphasizing the key issues between fabrication process and circuit design. There are three main conclusions from this review. First is the rapid progress toward low voltage operation such as 1.5-V, 64-Mb operation due to requirements of power reduction, scaled devices and battery operation. Second is the technology sophistication developed in the past decade resulting mainly from fine geometry patterning assisted by vertical structures. Third is the extended refresh time, that is, less cell leakage current is required with increasing memory capacity, as large as 64ms at 64Mb generation. Based on these results, it is predicted that power supply standardization, super low power, cell leakage current reduction and low-cost technologies pose continuing serious concerns for realizing deep sub-micron DRAMs.

1. INTRODUCTION

The density of DRAMs has quadrupled every three years since their introduction almost 20 years ago, and 64-Mbit DRAMs [1] [2] have already been developed. In addition to density increase, there are clear trends from recent reports toward low-voltage and low-power DRAMs permitting battery-operation [3] [4], and high-speed DRAMs such as 17-ns 4-Mb DRAMs [5] [6] and an exploratory 8-ns 4-Mb ECL BiCMOS DRAM [7]. To realize gigabit DRAMs, however, low voltage and high density are essential. In particular, more attention must be paid to the ever-increasing sophistication of chip technology and more severe requirement of refresh time.

In this paper, trends in DRAM technologies up to 64Mb are reviewed, emphasizing the above-described key issues between fabrication process and circuit design. Also, the prospects for these issues toward a gigabit era are discussed.

2. DRAM TECHNOLOGY TRENDS

(1) LOW VOLTAGE OPERATION To maintain the reliability of miniatured devices and to reduce power dissipation, low voltage operation [16] for traditional DRAM development is becoming essential. An external power supply Vcc of 5V has been maintained in the past decade ranging from 64Kb to 16Mb, followed by a 3.3-V Vcc for 64-Mb generation (Fig.1). Regarding internal operation, the operating voltage could be 5V until 4Mb because the maximum device operable voltage (Vopmax) was larger than 5V. The Vopmax is determined by the gate insulator reliability of the word-boosted cell transistor. At 16-Mb generation with a Vopmax of less than 5V, however, the operating voltage is reduced to 3.3 to 4V, while maintaining a Vcc of 5V with an on-chip voltage limiter (converter). The limiter is important to users to conserve the Vcc for several generations,

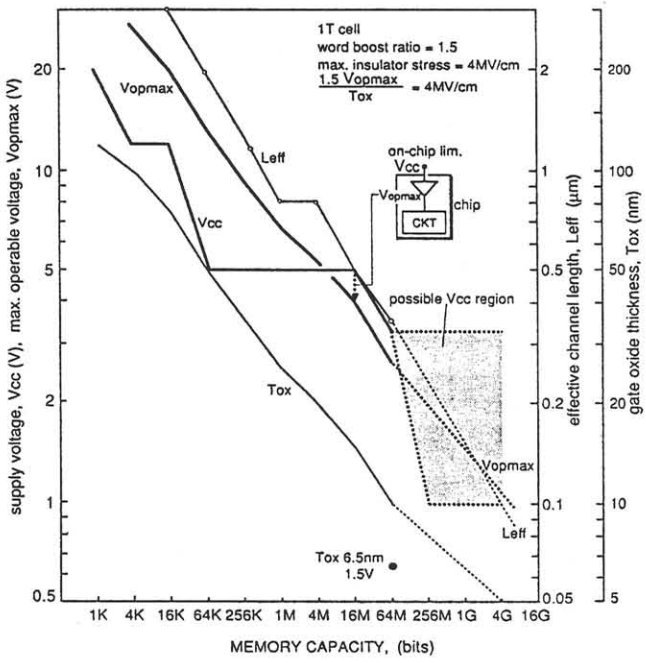

Fig.1 Trends in external power supply, maximum device operable voltage, and transistor size in periphery.

adjusting the internal voltage V_L in accordance with the ever-decreasing Vopmax to ensure device reliability. Recent concern has been on the accelerated burn-in test capability, because an well-fixed V_L at normal operation prevents from providing a sufficiently high stress voltage to internal circuit devices during a burn-in test, and thus from performing successful device screening. To solve this problem, a dual-regulator scheme [8] featuring a raised V_L during a burn-in test has been proposed (Fig.2). In this scheme, V_L is obtained by selecting the higher voltage between two voltages, V_{LN} and V_{LB}, while allowing equal stress conditions for both.

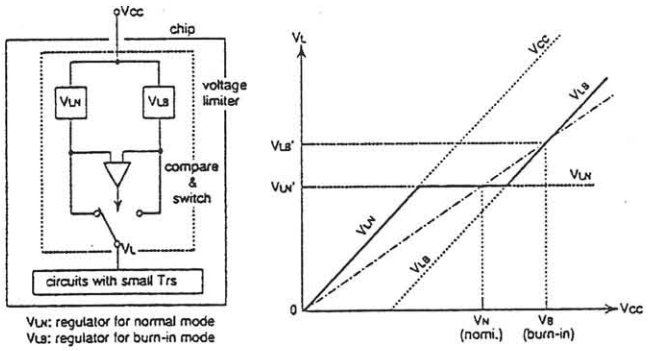

Fig.2 Burn-in test scheme for a chip using voltage limiter.

Recent activities for realizing long-awaited battery operation such as an experimental 1.5-V 64-Mb DRAM [1] are accelerating the trend in low voltage operation. In battery operation, the chip must be operated on a variety of batteries with various supply voltage levels under a long-term, supply voltage fluctuation due to battery characteristics. The universal-Vcc concept [3] is one good example for meeting this requirement. It features a 0.3-μm, 64-Mb core operable with a low voltage of 1.5V, which is generated by a voltage limiter. Suppression of the internal voltage fluctuation within 10% has been reported and thus offers an almost constant access time as fast as 50ns even when operated from a Vcc range of 1.5V to 3.6V. A battery-operated 4-Mb chip without an on-chip voltage limiter [4] is another example. An operating voltage as wide and low as 2.6± 1V has been realized with an access time of 190ns at Vcc = 1.6V. To relax the high-stress voltage applied to word lines at a high-voltage region, one of the dual word boosters is turned off. A refresh monitor cell is responsible for a stand-by current as low as 3μA with extended refresh-time operation.

(2) MORE SOPHISTICATED CHIP TECHNOLOGY Higher density and increased memory capacity make the technology choice more difficult. The most controversial issue is memory cell development (Fig.3). The state-of-the-art memory cell seen in the actually designed 64-Mb chips shows at least two new directions: advanced stacked cells [1] and stack-in-trench cells [2]. Almost all the stacked cells feature a storage node formed on the data-line. This allows the interference noise to be reduced with a shielded data-line structure. In addition, the stacked cells feature double-fin or crown-shaped storage node structures to increase the stored charge Qs. Even a higher dielectric constant of Ta_2O_5 is used. A stack-in-trench cell overcomes the cell leakage and α -induced charge collection issues, while maintaining the trench's advantages of obtaining large Qs and a relatively low step height. In any event, maximized Qs has been realized with additional complexity at each generation. This has resulted in a gradual decrease of Qs, despite a sharp decrease in cell area with increasing memory capacity.

The advancement achieved in the past decade is shown by a comparison between 64Kb [9] and 64Mb [1] (Table1 and Fig.4). The technology sophistication is mainly due to achieving high density. The degree in fine geometry patterning is relaxed only by adding vertical structures such

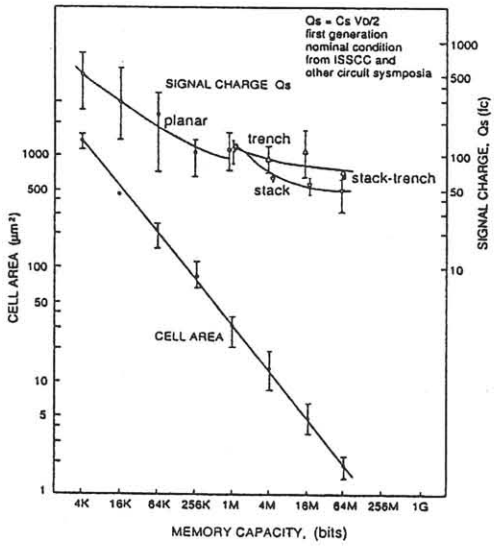

Fig.3 Trends in cell area and signal charge.

Table 1 Technology advances in the past decade [1] [9]

		64Kb (1980 ISSCC early production)	64Mb (1990 VLSI CIRCUIT SYMP. experimental)	CONTRIBUTIONS OF ADVANCEMENT
WAFER		4"	8" (expected)	cost
PROCESS		3 μm N-MOS double poly, single metal	0.3 μm triple well C-MOS double poly, single polycide, W plate triple metal	density density speed & density
Trs. (Leff / Tox)		2 μm / 50 nm	0.35 μm / 6.5 nm	density & speed
MEMORY CELL		144 μm², planar, Vcc plate	1.3 μm², stack, half Vcc plate	density (S / N) & power
	Cs /Co	38 / 515 fF	44 / 250 fF, shielded data line	
CIRCUIT		—— —— Vcc precharge double-divided data-line	redundancy (expected) parallel test half Vcc precharge multi-divided data line	cost cost power power & density
CHIP	AREA	26 mm²(3.43X7.52)	198mm²(9.74X20.28)	power & reliability
	POWER	5V	1.5V or 3.3V (on-chip limiter)	
	ACCESS	90 ns	50 ns	
	POWER	220mW (cycle 230 ns)	44mW (cycle 180ns, 1.5V)	battery use
	ORGANIZ.	64KWX 1bit	16MWX 4bit	ease of use
	REFRESH	2 ms / 128	64 ms / 8K	

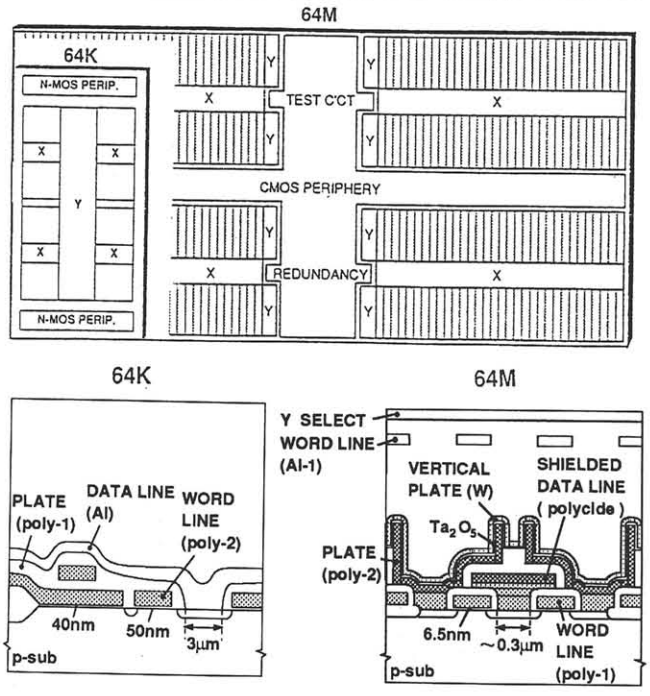

Fig.4 Comparisons of chip architecture and memory cell structure between 64Kb and 64Mb.

as multilayered wirings and crown-shaped stacked capacitor cells. Bisides larger wafer size, redundancy and parallel testing, this relaxation is a solution for realizing reasonable bit-cost despite resulting sophistication. A 1.5-V operation with high speed also necessitates developments of a higher cell capacitance and a thin gate insulator of 6.5nm.

(3) LONGER REFRESH TIME Refresh time (t_{REFmax}) has increased as memory capacity, that is, array matrix size **mn** (Fig.5) has increased, and is already as large as 64ms even at 64-Mb generation. Increasing t_{REFmax} with less cell leakage is essential to keep the performance loss γ as small as possible (Fig.6). Moreover, a further increased t_{REFmax}, if possible, provides the additional attractive features of less active current with smaller **m** and less stand-by current with an extended t_{REFmax}. Thus, reduced junction temperature Tj and suppressed leakage based on the micro-failure analysis of worse cells are important. To reduce Tj, the reduction of power dissipation in addition to both the package thermal resistance θ_{ja} and ambient temperature Ta is also important. For this reason, chip designers have attempted to reduce power dissipation as much as possible. The main contributors [10] to power reduction are low voltage operation, lower load capacitances through reduction of chip size, the almost doubling of the refresh cycle **n** at each generation, the CMOS half Vcc precharge, and the multi-divided data-line scheme.

3. PROSPECTS

In addition to high density and ultra-clean processes, special attention should be paid in the gigabit era to power supply standardization [10], super low power , cell leakage current reduction, and low-cost technologies. The issue of power supply standardization in the next decade is the most controversial, since it is completely different from that in the past. We are already faced with a serious situation that even a new standard of 3.3V is too high to be used for many years in deep-submicron LSIs. Furthermore, the low voltage requirement from the traditional DRAM approach, where higher density with the continually miniaturizing of devices is the first priority, might be merged with the voltage requirement from battery-operated handheld equipment. As a result, a plural number of standard voltages might coexist. In any event, the standard(s) will eventually set between 3.3V and 1V through serious discussion between makers and users, deeply affecting the development of deep-submicron technology. High breakdown voltage devices might be important to develop as long as they require acceptably simple fabrication processes. Whatever power supplies may be standards, an on-chip voltage limiter and something like the universal-Vcc concept despite their inherent power loss might be also necessary.

The key to super low power design is low voltage operation. Thus, increased Qs, reduced noise [10] and low-voltage sensing are vital. The non-scalable threshold voltage (V_T) issue is also one of the major concerns in realizing super low stand-by power while keeping high speed even for low voltage operation. This issue comes from the tailing

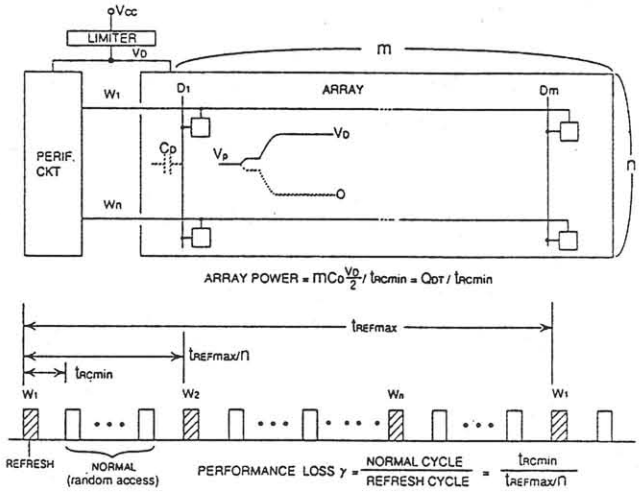

Fig.5 Refresh operation scheme.

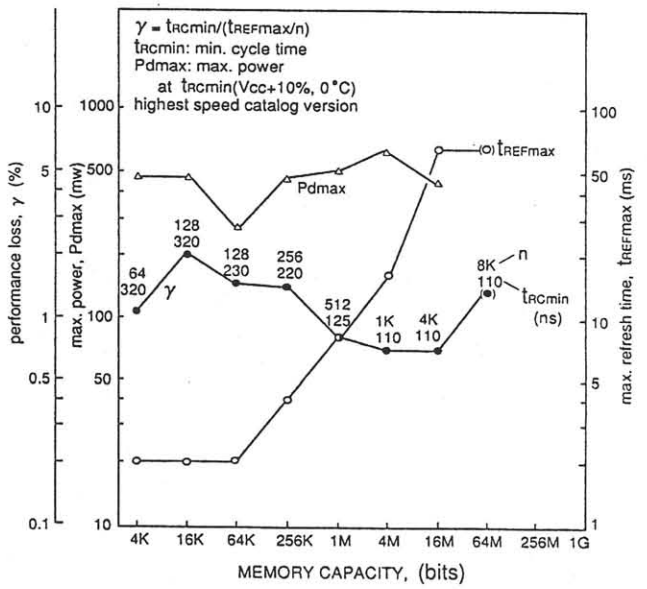

Fig.6 Trends in refresh time, refresh performance loss, and power dissipation.

characteristics of MOS transistors preventing V_T scaling without CMOS inverter penetrating current. The 64-Mb chip, stand-by current caused by CMOS inverters increases with decreasing V_T and increasing Tj (Fig.7). For example, the minimum V_T (V_{Tmin}) for a current of 10μA at Tj= 40°C suitable for a battery back up is 0.22V. V_{Tmin} is almost constant regardless of the degree of device scaling down, and V_T has a spread of ΔV_T. Hence, the speed is degraded as the operating voltage decreases according to the scaling, making the worst speed for the maximum V_T of $V_{Tmin} + 2\Delta V_T$. This implies that the 1V operation at high speed and a low stand-by current of 10μA is pessimistic. Hence, innovative MOSTs with low tailing coefficient and new CMOS circuits as well as reducing Tj must be developed to solve these issues.

Continually improving the refresh time is another concern, since a t_{REFmax} as long as 256ms is seemingly needed for 1Gb (Fig.6). Lowering Tj is essential to obtain a longer t_{REFmax}, as discussed previously. Its importance can be

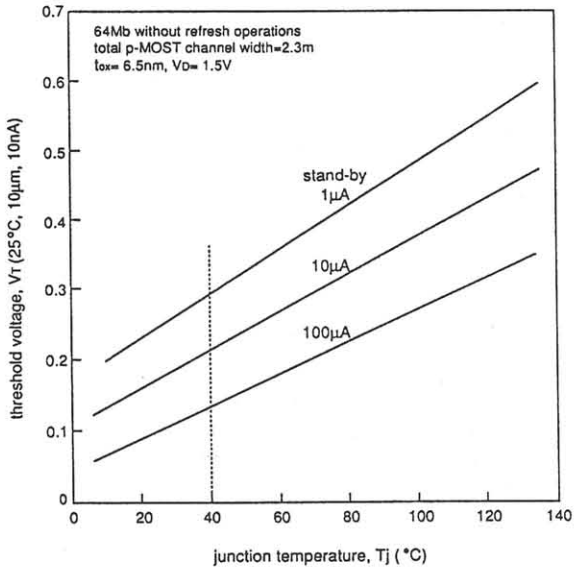

Fig.7 Threshold voltage versus junction temperature for a given stand-by current of a 1.5V 64Mb [1].

clarified by an example of power reduction (Fig.8). In this example, the same cell leakage density as in the 1-Mb cell is never developed without a power decrement of 0.12W at every generation. Even while keeping the same power, the 1-Gb leakage density increases by thirtyfold compared with that for 1Mb.

In terms of lowering the operating voltage and increasing the t_{REFmax}, a drastic reduction of Tj down to Liquid Nitrogen Temperature [17] is essential. However, device and circuit innovations permitting room temperature operation are still extremely important for widely used LSIs. Of course, reduction of power dissipation and θja through continuous improvement of conventional technology is vital as well.

Bit-cost reduction [11] is becoming more difficult due to increases in chip size, process-steps and manufacturing-cost. Thus, more cost-oriented DRAM developments should be emphasized so that the LSI industry thrives even in the gigabit era. Obviously, the key to this is the memory cell itself. New concepts surpassing the existing vertically structured cells in simplicity such as BORAM [12], multilevel storage DRAM [13] and planar cells using ferroelectric or high dielectric constant materials [14] [15] must be developed. Improved redundancy is also indispensable.

4. CONCLUSION

Progress in lowering operating voltage, sophistication of chip design, and more severe requirements of refresh time is continuing. Thus, power supply standardization, super low power, cell leakage current reduction and low-cost technologies are predicted to pose continuing serious concerns for realizing deep sub-micron DRAMs.

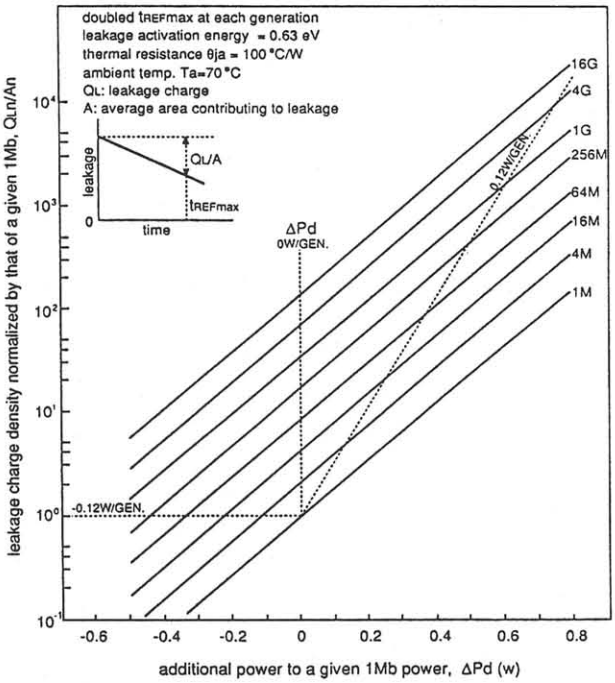

Fig.8 Sensitivity of cell leakage charge density to power dissipation.

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