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Tunnel Structured Stacked Capacitor Cell (TSSC) for 64 MBit dRAMs

N. Matsuo, Y. Nakata, H. Ogawa, T. Yabu, S. Matsumoto, M. Sasago and S. Okada

Semiconductor Research Center, Matsushita Electric Industrial Co., Ltd.
Yagumo-nakamachi, Moriguchi, Osaka 570, Japan.

A new 3-dimensionally (3-d) stacked capacitor, TSSC, was developed. The TSSC realized the improved reliability and a capacitance of 29 fF with 0.25 μm capacitor height because of the side-wall electrodes. The equivalent thickness of SiO_2 for the Oxide Nitride Oxide film (ONO) is 7.8 nm, and the cell area is 1.8 μm^2. The side-wall electrodes formation leads no generation of the local field concentration inside of the tunnel that are clarified by the Transmission Electron Microscopy (TEM) observation for the uniformity of the ONO inside of the tunnel. These results indicate that the TSSC is one of the potential candidates for 64Mbit dRAMs.

1. Introduction: 3-d stacked capacitors become essential to realize the high-density dRAMs [1,2,3,4]. There are several requirements. : (1) The reliability of the storage electrode which is closely related with the localized concentration of the electric field at the capacitor electrode and the uniform deposition of the capacitor-dielectric-film within the narrow gap of the storage electrode. (2) The optimum capacitor structure with large capacitance of which height is limited by the depth of focus of photo lithography (±1.0 μm; in case of KrF).[5] This paper proposes a new cell (TSSC) possessed of the above requirements and describes the reason of the improved reliability of this cell.

Figure 1.(a), (b) show a schematic view and the SEM photograph of the storage electrode of the TSSC with 2 tunnels, respectively. The storage electrode of the TSSC is composed of both the inner electrodes and the side-wall electrodes which are attached to the both sides of the inner electrodes to make the tunnels in the storage electrode. The reduction of the electric field concentration at the storage and plate electrode and a high capacitance with the small capacitor height can be realized. From a simple calculation, the capacitance of the TSSC is about 1.5 times as large as the stacked cell which is composed of only the inner electrode shown in Fig. 1(a).

2. Experimental procedure: The TSSCs with 1 tunnel or 2 tunnels and the STC were fabricated. The process sequence of the TSSC is shown in Figure 2. The cell area is

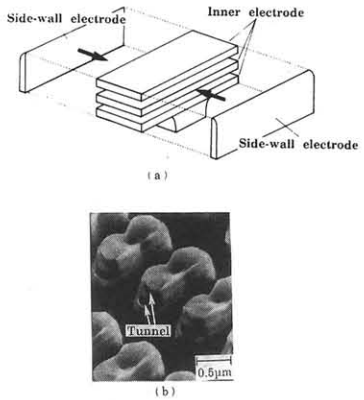

Figure 1. (a) a schematic view and (b) a SEM photograph of the storage electrode of the TSSC with 2 tunnels. The side - wall electrodes are attached to the both sides of the inner electrodes to make the tunnel in the storage electrode.

1.8 μm^2 and the tunnel height equal to the thickness of the SiO_2 (shown in Fig. 2(c)) is 50 nm for both TSSCs. The thickness of both the inner electrodes and the side-wall electrodes are 50 nm. The ONO consists of three-stacked layers: the natural oxide at the bottom, the intermediate nitride film which was grown by the LPCVD method, and the top oxide film by the wet method. The equivalent thickness of SiO_2 for ONO is 6-7.8 nm. The leakage current - plate voltage (I-V) characteristics, the distributions of the breakdown voltage, the constant voltage Time Dependent Dielectric Breakdown (TDDB) characteristics and the capacitances were examined for the TSSCs and the STC by measuring the 512K cell arrays. A positive bias was applied to the plate electrode. The breakdown voltage was defined as the bias at a leakage current of 1mA. The uniformity of the ONO inside of the tunnel was evaluated by observing some areas at regular interval from the opening

of the tunnel for the specimen of which tunnel length is 15.6 μm with Transmission Electron Microscopy (TEM). Figure 3 illustrates the relationship between the cross section, which is for the TEM observations both perpendicular to the tunnel and parallel to the tunnel, and the storage electrode.

3. Results and discussion: Figure 4 shows the results of the I-V characteristics at the positive bias, for the TSSCs and the STC. The leakage currents of the TSSCs with 1 tunnel or 2 tunnels and the STC are proportional to the capacitance area of these capacitors. At the negative bias, the leakage currents are smaller than that at the positive bias. Figure 5 shows the

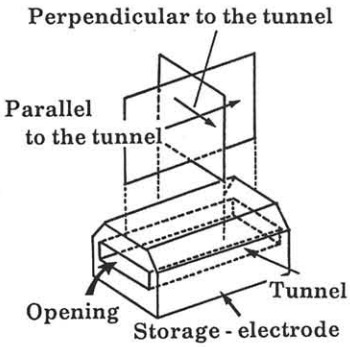

Figure 3. The relationship between the cross section, which is for the TEM observations both perpendicular to the tunnel and parallel to the tunnel, and the storage electrode.

results of the distributions of the breakdown voltage for the TSSCs and the STC. There was no degradation of the distributions of the breakdown voltage for the TSSCs, compared with the STC. Figure 6 shows the results of the TDDB characteristics for the TSSC with 2 tunnels and the STC. These datas are normalized by the capacitance areas. The characteristics of the TSSC is as same as that of the STC. These results indicate that the electric field concentration at the capacitor electrode is not generated for the TSSC. To clarify this phenomenon, the ONO inside of the tunnel was examined. Figures 7.(a), (b) and (c) show the cross sectional TEM photographs at the area of approximately 5 μm from the opening of the tunnel. Fig. 7(a) is perpendicular to the tunnel, and Fig. 7(b) is parallel to the tunnel. The ONO inside of the tunnel except for the corner of the tunnel is uniform over the entire length, and the thickness of which is as same as that outside of the tunnel. Fig. 7(c) is at the corner of the tunnel shown by the circle in Fig. 7(a). At the corner of the tunnel, the top oxide film (shown by "B") of the ONO is a little thicker than that at the other area, and the shape of the plate electrode at the corner of the tunnel is round. These shape effects are caused by the side-wall electrode formation. Because there is no generation of the local field concentration inside of the tunnel as shown in the schematic view of Fig. 7(c), the reliability of the TSSC is as good as that

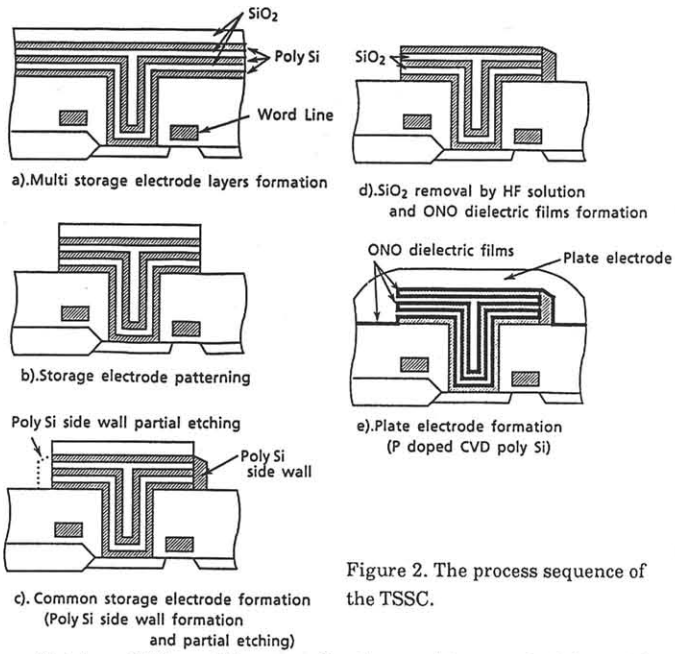

Figure 2. The process sequence of the TSSC.

of the STC. Figure 8 shows the relationship between the capacitance and the cell area. The TSSC realizes a capacitance of 29 fF (7.8 nm SiO_2 equivalent) and 0.25 μm capacitor height with 2 tunnels because of the side-wall electrode formation. The TSSC with 2 tunnels was applied to 64Mbit dRAMs. Figure 9 shows the cross sectional SEM photograph of 64Mbit dRAMs. Figure 10 shows the operation wave form. These

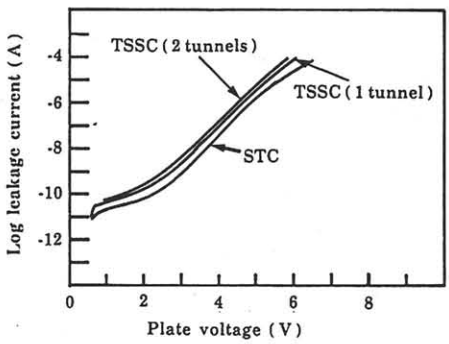

Figure 4. The I - V characteristics at the positive bias, for the TSSCs with 1 tunnel or 2 tunnels and the STC. The equivalent thickness of SiO_2 for ONO film is 6 nm.

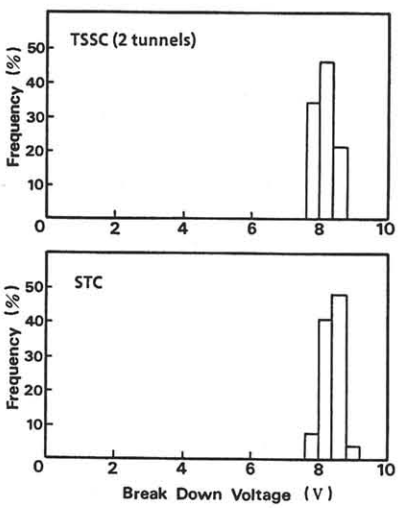

Figure 5. Distributions of the breakdown voltage for the TSSC with 2 tunnels and the STC. The equivallent thickness of SiO_2 for ONO film is 7.8 nm.

results indicate that the TSSC is one of the potential candidates for 64Mbit dRAMs.

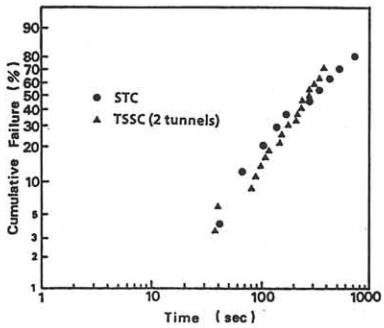

Figure 6. TDDB characteristics both for the TSSC with 2 tunnels and the STC under 6.75 voltage. The equivalent thickness of SiO_2 for ONO film is 7.8 nm. These datas are normalized by the capacitance areas.

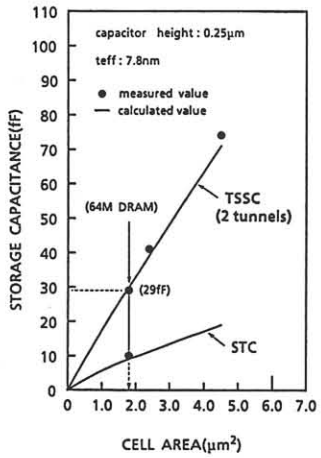

Figure 8. The relationship between the storage capacitance and the cell area. The TSSC with 2 tunnels realizes a capacitance of 29 fF. The cell area is 1.8 μm^2. The capacitor height is 0.25 μm.

4. Summary: The TSSC with 2 tunnels realizes (1)the same reliability as that of the STC, and (2)a capacitance of 29 fF with 0.25 μm capacitor height which are both because of the side-wall electrode formation. The ONO inside of the tunnel was uniform except for the corner. The thickness of the ONO is a little larger at the corner and this phenomenon leads the improved reliability.

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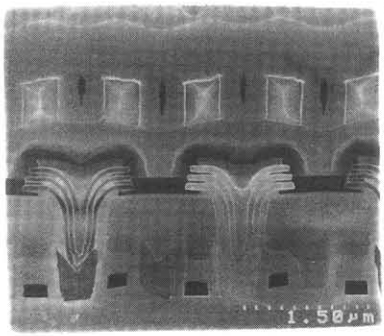

Figure 9. The cross sectional SEM photograph of 64Mbit dRAMs.

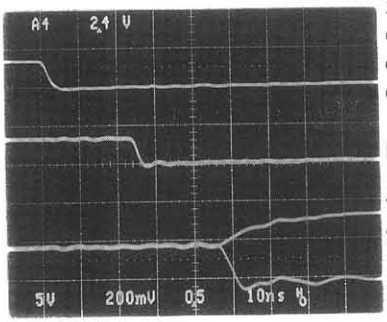

Figure 10. The operation wave form.

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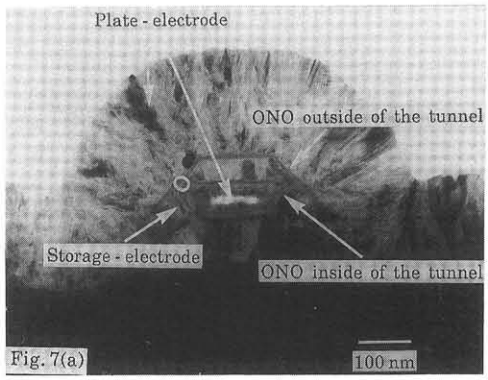

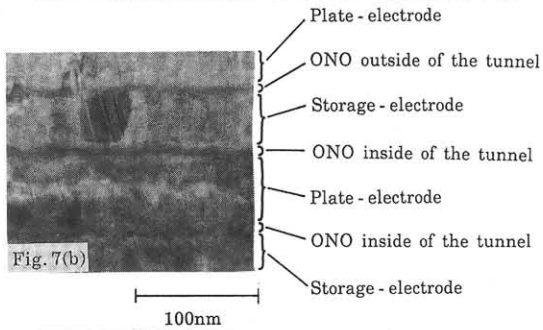

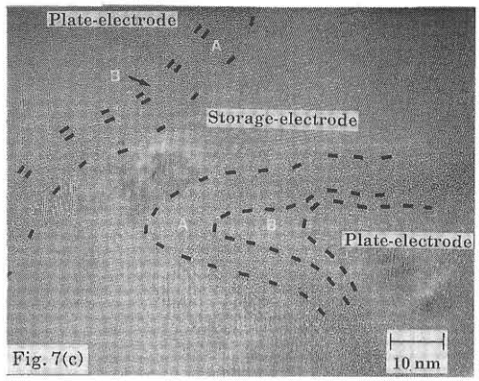

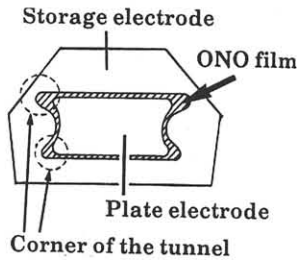

Figure 7. The cross sectional TEM photographs of the TSSC with 1 tunnel and the schematic views of it. Fig. 7(a) is perpendicular to the tunnel and fig. 7(b) is parallel to that. Fig. 7(c) is at the corner of the tunnel shown by the circle in fig. 7(a). The area shown by "A" is the 2-layer film composed of the nitride and the bottom natural oxide, and the area by "B" is the top oxide. The schematic view both of the ONO and the plate - electrode inside of the tunnel is added to Fig. 7(c).