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An Advanced Fabrication Technology of Hemispherical Grained (HSG) Poly-Si for High Capacitance Storage Electrodes

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A new fabrication technology, in which an even-surfaced amorphous-Si electrode is changed into an uneven surface of hemispherical grained Si (HSG-Si), is developed for realizing 64Mbit DRAMs. This fabrication method consists of easily-controllable processes: formation of smooth-surface amorphous-Si electrodes followed by native oxide removal and high vacuum annealing. In this process, HSG-Si is formed by nuclei generation on the amorphous-Si surface and by outward crystalline growth of grains. By using the high-vacuum annealing process for HSG-Si fabrication, the surfaces of storage electrodes of all types can be covered with HSG-Si, thus increasing their surface areas by a factor of 1.8. Such an increase makes it possible to reduce the height of storage electrodes through the use of relatively thick dielectric films which have higher reliability. This technique is applicable to the fabrication of 64Mbit and larger DRAMs.

I. INTRODUCTION

In the down-scaling of DRAM cells, an advanced storage capacitor fabrication process is required to provide sufficiently large capacitance in a limited area, and enlargement of the surface of storage electrodes is one of the most effective approaches to meeting this requirement. One recent approach to increasing surface area has been the development of a technique for fabricating uneven Si film surfaces. Low-pressure chemical vapor deposition (LPCVD) was used to produce a hemispherically grained (HSG) Si surface, and this proved to be an efficient technique for surface area enlargement[1-5]. Its application to DRAM processes, however, has involved significant difficulties.

First, strict temperature control is required to deposit uniform HSG-Si films[1-3),5)], and when, after LPCVD, the excess HSG-Si to either side of a storage electrode is etched off, the areas at its foot are left flat[4)]. Further, when applied to cylindrical storage electrodes, even more of the advantage is lost because HSG-Si is not formed on the inner walls of the cylinder.

In the present work, we have developed a new technology in which an even-surfaced amorphous-Si electrode without native oxide is changed into an uneven surface of HSG-Si through simple high-vacuum annealing[6)]. With this technique, surfaces of any type of storage electrode can be entirely covered with HSG-Si to effectively increase their surface areas.

II. EXPERIMENTS

In the LPCVD method for HSG-Si fabrication, Si films were deposited on SiO_2/Si substrates. Deposition was carried out with He-diluted SiH_4 (20%) gas at 1.0 Torr pressure at 590°C, measured at the wafer surface, using an infrared thermo meter. After deposition, Si films were maintained in a vacuum at deposition temperature for various time periods. In our high-vacuum annealing method, LPCVD amorphous-Si films with completely flat surfaces were deposited at 550°C on SiO_2/Si substrates which had contact holes. The amorphous-Si for storage electrodes was patterned by lithography and reactive ion etching (RIE). Native oxides on the electrodes were removed by etching with diluted HF solution. Annealing of amorphous-Si electrodes was performed in a high-vacuum annealer in which the process pressure was $1x10^{-7}$ Torr.

Reflection high energy electron diffraction (RHEED) was used to judge the crystallinity of Si electrode surfaces. The surface morphologies of the deposited Si films were observed by scanning electron microscopy (SEM).

The surface areas of the deposited Si films were estimated by measuring the capacitance values of stacked capacitors whose electrodes were made of the Si films. The Si-films were doped by thermal phosphorus diffusion. SiO_2/Si_3N_4 double layer films having 7nm SiO_2-equivalent thickness were employed as capacitor dielectric films. Upper electrodes were poly-Si deposited by LPCVD at 600°C, and this was followed by thermal phosphorus diffusion.

III. RESULTS

It has previously been reported by the authors that LPCVD formation of HSG-Si occurred at that temperature at which the film structure changed from amorphous to polycrystalline. In the present work, Si films were maintained in a vacuum at this transition temperature, i.e. the deposition temperature, even after deposition. Figure 1 shows SEM photographs of Si film surface morphology for various holding times in a vacuum after 590°C deposition. At 2 minutes, HSG-Si density is low and much of the surface is even, amorphous-Si. As the period of vacuum maintenance is increased, HSG-Si density increases. This shows that the HSG-Si is formed not during deposition but under annealing in the vacuum.

In our present research, we have attempted to study the HSG-Si annealing growth mechanism on a flat-surface amorphous Si film. After native oxide removal by a diluted HF solution, the amorphous Si surface was annealed in a vacuum. Figure 2 shows a cross-sectional TEM view of a Si film which had been annealed until the hollow RHEED pattern indicating an amorphous surface turned into the ring pattern which indicated a polycrystalline surface. The TEM micrograph shows that, even though hemispherical grains of crystalline are formed on the surface, an amorphous Si layer still exists under the HSG-Si. It is also seen that the HSG-Si protrudes from the original amorphous-Si plane, and that the amorphous Si surface sinks in around the HSG-Si. This indicates that HSG-Si was formed by migration of surface Si atoms and the crystallization of surface regions on the amorphous Si film. In contrast to native-oxide-free surfaces, amorphous Si films with native oxide maintained completely flat surfaces under annealing. This suggests that native oxide on amorphous Si surfaces suppresses Si atom migration and disturbs the HSG-Si formation. The high-vacuum annealing method for HSG-Si fabrication does not require the strict temperature control which was necessary in the LPCVD method. HSG-Si will simply form at that point at which rising temperatures pass through the 600°C mark.

SEM photographs in Fig.3 show practical examples of the high-vacuum annealing effects on surface morphology. Two types of amorphous-Si storage electrodes with even surfaces, a conventional one and a cylindrical one, were annealed in vacuum. After annealing, HSG-Si covered the entire surfaces of both types, including the inside walls of cylinders and any side walls which had previously been dry-etched. A surface area enlargement ratio of 1.8 was calculated by measuring the capacitance of capacitors of 7nm SiO_2-equivalent thick SiO_2/Si_3N_4 dielectric films.

Figure 4 shows storage capacitance estimates for four types of stacked capacitors. Their sizes and dielectric film SiO_2-equivalents are defined so as to be suitable for practical 64Mbit DRAMs. A capacitance of 40fF can be stored with a HSG-Si covered

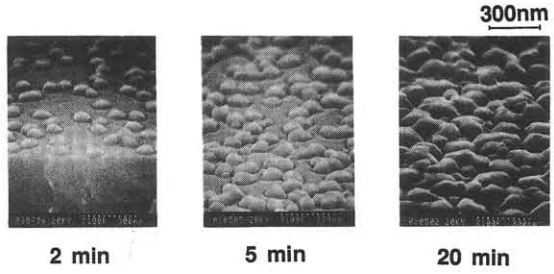

Fig.1 SEM photographs of Si film surface morphology depending on the holding time after deposition in a vacuum at 590°C.

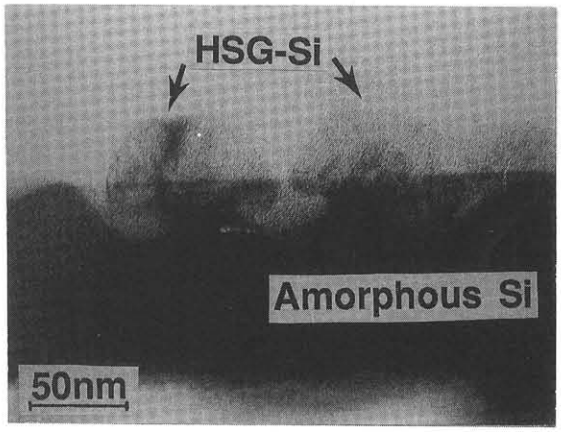

Fig.2 Cross-sectional TEM micrograph of a Si film annealed in a high vacuum.

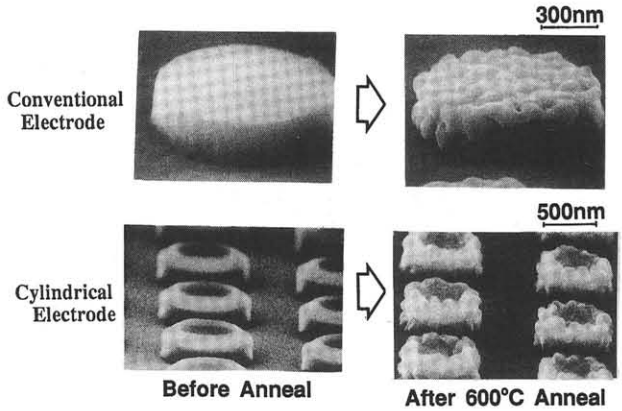

Fig.3 SEM photographs of two types storage electrodes before and after high-vacuum annealing.

cylindrical electrode formed by the high vacuum annealing method, which is clearly superior to the LPCVD method in storage-electrode surface area enlargement.

Figures 5(a) and 5(b) show the current-electric field characteristics of SiO_2/Si_3N_4 composite films formed on HSG-Si electrodes made by the annealing method, in contrast with those for conventional polycrystalline Si electrodes. A comparison of Figs. 5(a) and 5(b) indicates that the leakage current increase caused by HSG-Si unevenness is negligibly small. Figure 6 shows breakdown-field distributions formed on a HSG-Si electrode which was made by the annealing method. The peak of the breakdown-field distribution is sharp and no breakdown failure in low electric fields is observed.

VI. CONCLUSION

We have developed a new technology for producing high-capacitance storage electrodes using an advanced process for forming uneven electrode surfaces of HSG-Si. The new HSG-Si fabrication method consists of easily-controllable processes: formation of smooth-surface amorphous-Si electrodes followed by native oxide removal and high vacuum annealing. This high-vacuum method for HSG-Si fabrication is greatly superior to the previously-reported HSG-Si fabrication method, which needs strict temperature control during LPCVD and which can not be applied over entire electrode surfaces. With the new process, for the surfaces of storage electrodes of all types can be covered with HSG-Si, increasing their surface areas by a factor of 1.8. Such an increase makes it possible to reduce the height of storage electrodes through the use of a relatively thick dielectric film which has higher reliability. This technique is applicable to the fabrication of 64Mbit and larger DRAMs.

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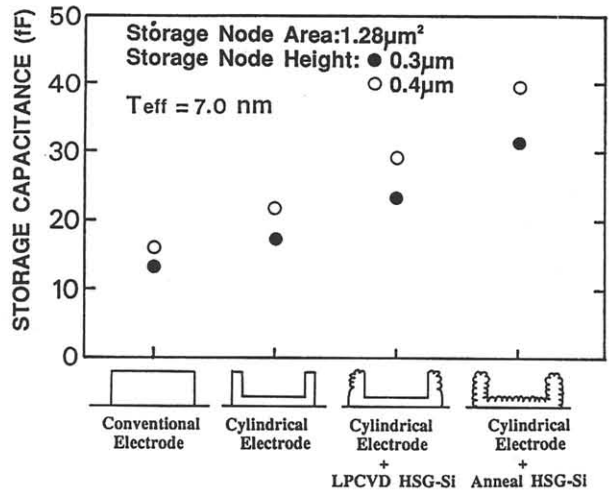

Fig.4 Storage capacitances for various electrode structures for 64Mbit DRAM.

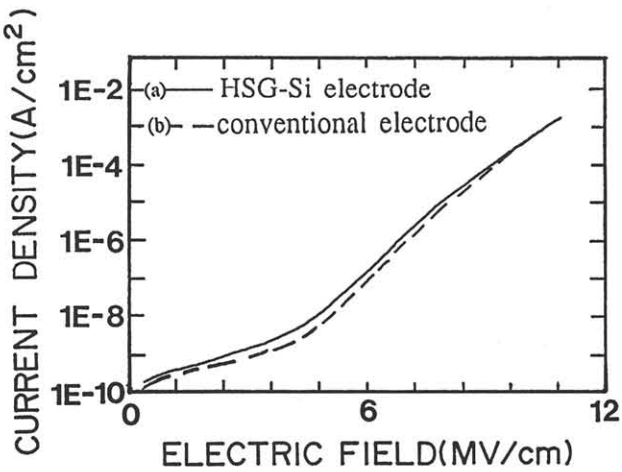

Fig.5 I-E characteristics of 7nm(Teff)-SiO_2/Si_3N_4 dielectric films formed on annealing-method HSG-Si electrodes and conventional electrodes.

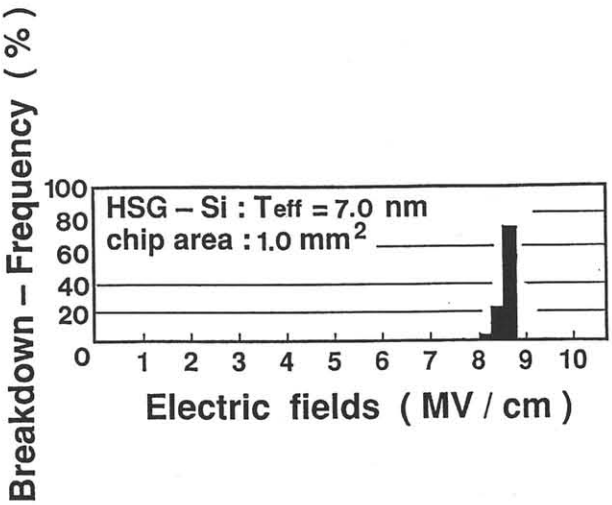

Fig.6 Breakdown field distribution of Teff=7nm(Teff)-SiO_2/Si_3N_4 films on annealing method HSG-Si electrodes.