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An Analysis of p^+-n Junction Capacitance with Three-Dimensional Impurity Profiling Method Using Scanning Tunneling Microscopy

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A p^+-n junction capacitance characteristics has been analyzed with a novel three-dimensional impurity profiling method using chemical etching and scanning tunneling microscopy. The calculated capacitance-voltage characteristics for plane and sidewall capacitances agree better with the measured characteristics compared to that obtained with conventional SIMS analysis. It was found that the C-V characteristic for sidewall capacitance scarcely depend on the impurity profile. The proposed STM profiling method will be a promising tool for a device characterization for nanometer-scale ULIs.

1. Introduction

To realize high density and high speed ULSIs, it is very important to obtain accurate intrinsic and parasitic device parameters including those of passive elements. Although characteristics of interconnection line capacitance have widely been investigated,[1] little is known about characteristics of p-n junction capacitance. This is because accurate impurity profiles, including lateral profiles, could not be measured with conventional impurity profiling methods. A new secondary ion mass spectrometry(SIMS) measurement[2] capable of two-dimensional impurity profiling has been developed, but the lateral resolution is 0.5μm at best. Scanning tunneling microscopy(STM) and related technologies have been used as microcharacterization tools for processes and devices because of their high resolution. Lateral dopant profiling was realized with scanning capacitance microscopy technique, but the resolution is 0.2μm.[3]

Recently we have proposed a novel three-dimensional impurity profiling method with 10nm resolution which comprises etching a cleaved silicon surface of boron implanted layer and imaging the etched surface by STM.[4] In this paper, we demonstrate that capacitance-voltage(C-V) characteristics of p^+-n junctions are well analyzed using this profiling method.

2. Novel impurity profiling method

Fig. 1 shows schematic drawing of the proposed impurity profiling method. The procedure is as follows. The sample is coated with resist material to prevent surface etching. The sample is then cleaved to expose a cross section through the implanted region. The cleaved surface is etched using an etchant whose etch-rate depends adequately on impurity concentration. Finally the resist is stripped and the etched surface is STM imaged in an air ambient.

The etching profile obtained from the STM image yields two-dimensional impurity concentration profile. A calibration curve between etched depth and the impurity concentration of reference samples with known impurity content is used for the conversion. The best etchant system has composition of HF, HNO_3 and H_2O with a volume ratio 1:100:25. The etchant is applicable to samples with a dopant range of 10^{16}-10^{20} cm^{-3}. Comparisons to depth profiles obtained with SIMS and spreading resistance methods reveal that this proposed method measures activated boron impurity concentration rather than total boron concentration. Three-dimensional profiling is possible with repeating the etching and STM imaging procedure.

3. Experimental Procedure

Impurity profiling and C-V characteristic measurements were

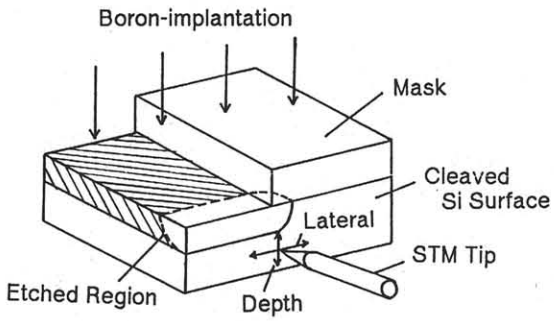

Fig. 1 Schematic drawing of the proposed implant dopant profiling method using STM.

performed with boron ion implanted n-type($n=5\times10^{16}cm^{-3}$) Si (100) substrate with a dose of $1\times10^{15}cm^{-2}$ at an energy of 70keV. Impurity profiles were measured using the profiling method described in Section 2 and SIMS. The C-V characteristics measurements of p^+-n junctions were carried out on different sizes using an impedance analyzer(HP4194A) at a frequency of 100MHz. Care was taken to insure that the measurements were carried out at a high enough frequency to obtain reproducible C-V characteristics. For the analysis of C-V characteristics, we used a two-dimensional device simulator(TRANAL).[5] Both measurements and calculation were carried out for bias voltage between 0V and 1V, because it is important to know low-voltage C-V characteristics for designing ULSIs with low supply-voltage.

4. Impurity profiles

The measured depth and lateral boron impurity concentration profiles using STM and SIMS depth profile are shown in Fig. 2. It is found that the junction depth obtained with STM is smaller than that with SIMS. Moreover, in this sample, lateral junction depth is determined as 70% of junction depth with 10nm resolution, while it is generally assumed as 60%-80% when designing MOS LSIs.

Fig. 3 compares two-dimensional impurity profiles obtained with the two methods. For SIMS data, we assumed lateral profile to be the same as depth profile and neglected the high concentration region which mainly contains electrically inactive impurity.[6] The distinct difference is depicted in the sidewall region which is away from implantation mask edge ; depth profile obtained with STM is gradual compared to SIMS depth profile, contrary to the depth profile in the plane region. The profile shows

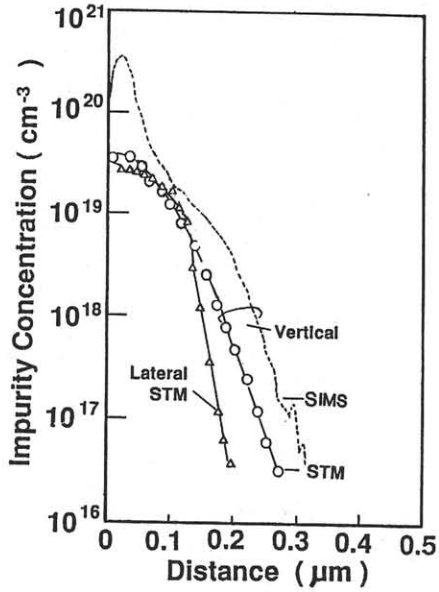

Fig. 2 Impurity concentration profiles. Lateral profile was measured beneath the mask starting from the edge.

almost straight-line impurity distribution just like that for linearly graded junctions. Thus, this nanometer-scale profiling method has first enabled us to analyze C-V characteristics of sidewall capacitance as will be described in the next section.

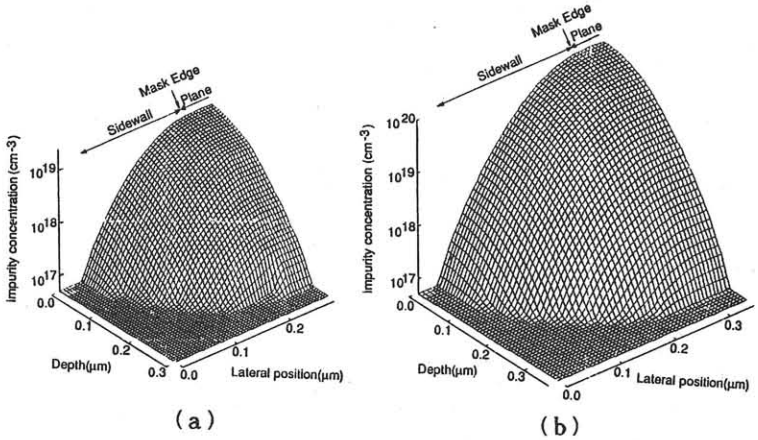

Fig. 3 Two-dimensional impurity profiles obtained with (a)STM and (b)SIMS.

5. C-V characteristics

C-V characteristics were calculated for the obtained impurity profiles with STM. The results for plane and sidewall capacitances are shown by solid lines in Fig. 4. Here, the applied voltage Va dependence of capacitance is evaluated using the following expression

$$C=Co(1+Va/Vbi-(2kT/q)/Vbi)^{-n}, \quad (1)$$

where Co is a constant, Vbi built-in voltage and k Boltzmann constant. The voltage dependence factor n is

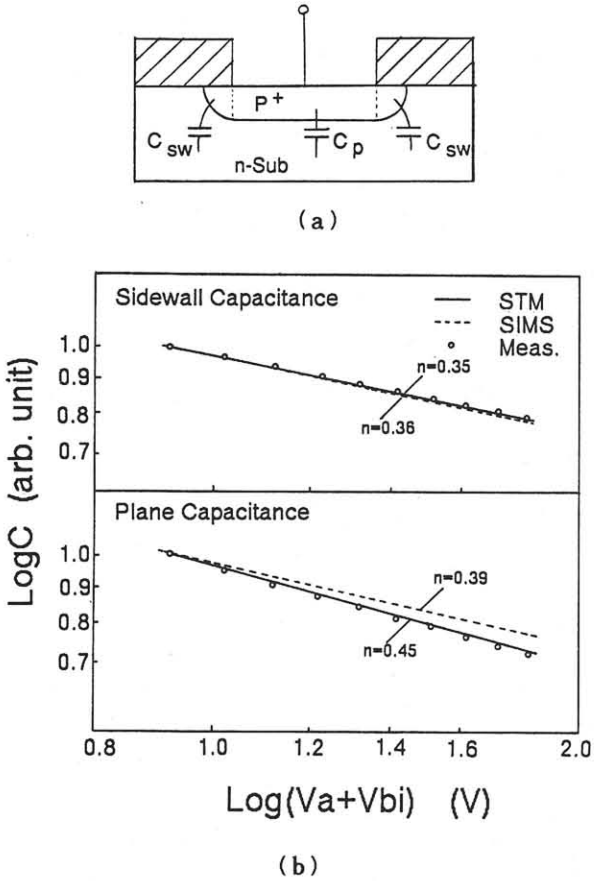

Fig. 4 (a) Cross-sectional view of p^+-n junction. Cp is plane capacitance and Csw is sidewall capacitance. (b) C-V characteristics. n is voltage dependence of capacitance described in Eq. (1).

extracted from the fitting to Eq. (1). The n for plane capacitance is found to be 0.45 and that for sidewall capacitance is 0.35.

The measured C-V characteristics are also shown by open circles. The agreement of calculated data with the measured results is remarkable. Also, the measured C-V characteristics difference between side wall and plane capacitance is also reproduced by the calculation. The n for sidewall capacitance is as small as that for linearly graded junctions (n=0.33). This is because an equivalent circuit for sidewall capacitance is expressed as parallel capacitors and hence C-V characteristic is dominated by that in the low surface impurity region where depth profile is almost straight-line impurity distribution.

Calculations were also performed for SIMS profile shown in Fig. 3(b). The results are shown in Fig. 4. The voltage dependence of plane capacitance (n=0.39) shows poorer agreement with the measured results compared to the calculated results for STM profile, because SIMS depth profile is gradual compared to STM profile. On the contrary, the voltage dependence of sidewall capacitance (n=0.36) is almost the same as that with STM profile. This is attributed to the fact that C-V characteristics are dominated by the region where depth profiles show almost straight as described above.

5. Conclusion

C-V characteristics of p^+-n junction have been evaluated using the STM profiling method which gives activated impurity profiles with nanometer resolution. It is demonstrated that calculated C-V characteristics for plane and sidewall capacitances show better agreement with the measured characteristics compared to that with SIMS profile. It was found that C-V characteristics for a side-wall capacitance scarcely depend on the impurity profiles. Moreover, the obtained capacitance value enable to simulate circuit performance more accurately, though not shown in the text. Thus, the proposed STM profiling method will be a promising tool for a device characterization for nanometer-scale ULIs.

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