Arithmetic Logic Circuits Using Resonant-Tunneling Hot Electron Transistors (RHETs)

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This paper describes new RHET arithmetic logic circuits, including a 3-input exclusive-OR gate and a 3-input majority logic gate. Using these 3-input logic gates, we have designed an RHET full adder. We confirmed the performance of the full adders using InGaAs/In(AlGa)As RHETs at 77 K. By using these RHET logic, the number of transistors was reduced by 1/4.

1. INTRODUCTION

In 1970, Esaki et. al\(^1\) proposed semiconductor superlattice called an artificial semiconductor crystal. They fabricated the crystal with MBE and measured its new electrical and optical characteristics, making new devices possible. In 1974, Chang et. al demonstrated that a resonant-tunneling phenomenon occurred in the artificial semiconductor crystal. However, at that time, the current peak-to-valley ratio was about 1.1, not good enough for device applications\(^2\). In 1983, Sollner et. al demonstrated the existence of resonant-tunneling barriers used for microwave applications, which exhibited an extremely large peak-to-valley ratio\(^3\). In 1985, Yokoyama et. al proposed and demonstrated a three-terminal resonant-tunneling devices, called the resonant-tunneling hot electron transistor (RHET) using a GaAs/AlGaAs heterostructure with possible uses in digital IC applications\(^4\). Although RHETs are just one of the devices in the family of hot electron transistors (HETs), proposed by Heiblum in 1981\(^5\), by applying a resonant-tunneling barrier as a hot electron injector, introduces possibility of new function devices. Since RHETs have a negative collector conductance with respect to the base-emitter voltage, they have many attractive characteristics for use in integrated devices. We previously demonstrated that RHETs reduce the numbers of transistors needed for IC, although the current gain was not high enough\(^6\). In 1988, we had developed an RHET using InGaAs/In(AlGa)As heterostructures, which had a higher current gain and emitter current peak-to-valley ratio\(^7\).

Recently in 1990, we further improved RHET performance by enhancing the collector current saturation voltage through a decrease in the thickness of i-In(AlGa)As collector barrier. We are now ready to fabricate useful integrated circuits.

2. 3-Input Logic Family

Previously, we designed and fabricated a 2-input logic family consisting of a 2-input NOR gate, a 2-input exclusive-NOR(E-NOR) gate, and a state holding circuit using RHETs\(^8\). Since the E-NOR gate uses its negative collector conductance effectively, only two transistors are needed. This is about one fourth the number needed as devices constructed of conventional transistors. We demonstrated a latch circuit as an example of a sequential logic circuit using an E-NOR gate and a state holding circuit. We were able to reduce the number of transistors by 1/2.

![Figure 1 Circuit diagram of a 3-input E-OR gate](image)

Now we introduce a new family of 3-input arithmetic logic circuits. Figure 1 diagrams a 3-input Exclusive-OR gate using RHETs. This gate uses two 2-input E-NOR gates. Since, as mentioned before, the 2-input E-NOR gate...
needs only two RHETs, we need only 4 RHETs and 8 resistors to construct the 3-input E-OR gate. This gate will be useful for the summation of a full adder.

Figure 2 shows a 3-input majority logic gate and the emitter-base current-voltage characteristics of RHET-1. The 3-input majority logic gate was constructed using 3 RHETs and 5 resistors. When either one or no inputs are high, the operating point of RHET-1 is not in the negative conductance region. When two or three inputs are high, the operating point is in the negative conductance region. RHET-2 inverts and increases the logic margin. The negative conductance region also increases the logic margin. So, this gate outputs the inverse of the majority of the inputs, which are useful in forming the carry signal in a full adder. The gate has one-sixth the number of transistors needed for a conventional implementation.

Figure 2 Circuit diagram and operation point chart of a 3-input majority gate

3. Structures of RHETs for IC fabrication

Figure 3 diagrams the RHET structure used in circuit fabrication. The RHET uses an asymmetric In$_{0.52}$Al$_{0.48}$As/In$_{0.53}$Ga$_{0.47}$As/AlAs (6.45 nm/2.93 nm/2.37 nm) resonant-tunneling barrier (RTB). The high AlAs barrier height and relatively narrow well width increases the logic-level difference of 3-input majority logic gates by separating the first and second resonant-tunneling levels. The base layer consisted of a 30-nm-thick n-In$_{0.53}$Ga$_{0.47}$As doped at a concentration of 1 X 10$^{18}$ cm$^{-3}$. The i-In$_{0.52}$(Al$_{0.5}$Ga$_{0.5}$)0.48As collector barrier was deposited 50 nm-thick to decrease the collector-current saturation voltage. A 300-nm-thick i-In$_{0.53}$Ga$_{0.47}$As layer was inserted between the collector barrier and collector channel to increase the base-collector breakdown voltage. Figure 4 shows the common-base collector current-voltage characteristics of this RHET as measured at 77 K. The common-base current gain was around 0.9 and the base-collector breakdown voltage was about 2.8 V. Figure 5 shows the emitter current as a function of base-emitter voltage at a $V_{ce}$ of 2 V. The peak emitter current density was 1.7 X 10$^4$ Acm$^{-2}$ at a base-emitter voltage of -0.72 V. Emitter and base electrodes were self-aligned using a SiO$_2$ side wall to reduce the base resistance. In IC fabrication, reactively sputtered WSiN thin film was used for the resistors.
4. Full Adder using RHETs

Figure 6 shows circuit diagram and micrograph of a full adder using RHETs. The full adder is constructed using a 3-input E-OR gate and a 3-input majority logic gate, for a total of 7 RHETs and 13 resistors. Our circuit has 3 inverters, one for each input A, B, and carry (C\text{\textsubscript{1}}) to increase the fan-in. It also contains 2 inverters for the sum (S) and carry (Co) signals to increase the drivability for the next stage. In this circuit, the 3-input E-OR gate sums the inputs. The 3-input majority logic gate calculates the carry. Figure 7 shows the operation of the full adder at 77 K with a supply voltage of 3 V. We confirmed that the full adder operated correctly. Note the number of transistors is one quarter and the supply voltage is one half compared to that of ECL logic circuits using InGaAs/InAlAs HBTs. Considering importance of reducing the delay time due to wires connecting transistors and intrinsic transistor speed, use of new functional devices such as RHETs offers the possibility of surpassing the speed limitation of conventional ICs. Since the full adder is the principle circuit in arithmetic logic circuits for computers, our results indicates a great potential for applying RHETs to future high-speed, low-power logic systems.

5. Summary

We proposed new RHET arithmetic logic gate family and designed a 3-input E-OR and a 3-input majority logic gate. Using these gates and our InGaAs/In(AlGa)As RHETs, a full adder was designed and fabricated as a principle building block for arithmetic logic units. We confirmed the full adder's correct operation at 77 K. This adder reduces the number of transistors to one quarter and the supply voltage to about one half as compared to the conventional bipolar transistors. These results indicated the possibility of decreasing the number of transistors while increasing the information processing speed using low-power RHETs in the new logic circuits.

Acknowledgment

This work was performed under the management of R&D Association for Future Electron Devices (PED) as a part of R&D of Basic Technology for Future Industries sponsored by the New Energy and Industrial Technology Development Organization (NEDO).

References