Extended Abstracts of the 1991 International Conference on Solid State Devices and Materials, Yokohama, 1991, pp. 92-94

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Sub-Quarter Micron Gate Fabrication Process Using Phase-Shifting-Mask for Microwave GaAs Devices

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Phase-shifting mask technique using i-line stepper was applied to the gate formation process of AlGaAs/GaAs HEMTs. To obtain a fine gate pattern less than quarter micron, the phase-shifter edge-line mask, which has the highest resolution and wide focus margin for isolated pattern, was used, and the double exposure process was developed to form a real gate pattern. The controllable gate length was in the range of 0.15-0.35μm. By using this technique, 0.18μm gate HEMTs with excellent microwave performances were obtained with high uniformity in a 3-inch wafer. This technique has the great advantages for microwave GaAs devices and ultra high speed GaAs LSIs.

1. Introduction

Sub-quarter micron gate GaAs devices have been developed for microwave communication and ultra high speed signal processing. Controllability of the gate formation process is the most important factor dominating transconductance, cut off frequency and noise figure of these devices. Electron beam lithography has been investigated to form sub-quarter micron gate. On the other hand, optical lithography using reduction projection exposure system still has the advantages of adoptability of the conventional technique and its high throughput.

To improve resolution and depth of focus, phase- shifting mask technique in optical lithography has been developed and used for sample production of 64M and 256M DRAMs. The principle of this technique is the interference between the light waves through transparent parts and waves through adjacent transparent parts with 180° phase-shifting. As a result, the light intensity at the boundary is reduced and the light contrast is improved. Among various phase-shifting mask methods[1-3], the most fine line can be patterned with the phase-shifter edge-line (PEL) mask [3]. This method is suitable for isolated pattern as gate electrode and is easy to design the mask pattern, because the edge of shifter pattern is utilized and the neighboring chrome pattern is not used in the mask. We applied this technique to the fabrication of sub-quarter micron gates of HEMTs and GaAs MESFETs for the first time and obtained good performance with high uniformity.

In this paper, we describe the PEL mask method using negative working resist LMR-UV (low molecular weight resist for UV lithography)[4], the double exposure process to form the gate pattern of microwave devices, and the device performance.

2. Resolution of the Phase-Shifter Edge-Line Mask Method

Fine space pattern for gate electrode was patterned in negative working resist (LMR-UV) using a 0.42NA i-line stepper (coherence factor of 0.5) with a PEL mask[3]. EB resist was used as a phase shifter on the PEL mask. The thickness of the shifter layer was set to about 350nm for 180° phase-shifting. Figure 1 shows the clearly resolved 0.2μm space profile with high aspect ratio. We describe the space width of developed resist as a resist space length, which corresponds to the gate length of devices. Since LMR-UV has a large absorption coefficient of 3.8μm^{-1} at i-line, overhung profile was formed with the taper angle of 80°. This properties is suitable for metal lift-off process which is commonly used in GaAs device process. The open circles in Figure 2 show the relation between the exposure dose and the space length patterned on the 0.7μm thick LMR-UV resist on GaAs substrate. The space length was controlled in the range

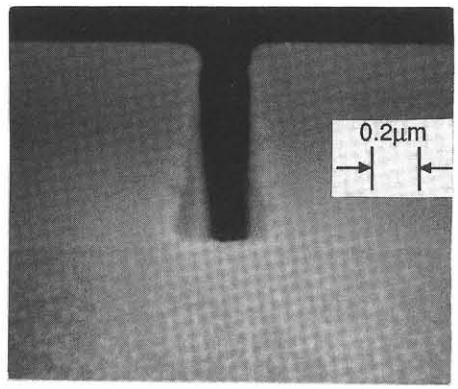

Fig.1 0.2μm LMR-UV space profile formed by using the PEL mask and the i-line stepper.

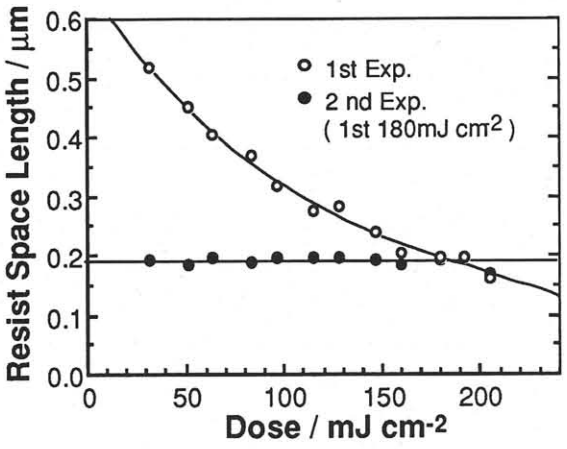

Fig.2 (○) Relation between 1st exposure dose and space length of 0.7μm thick LMR-UV resist, (●) relation between space length and 2nd exposure dose with additional mask in Fig.4(c) at a constant 1st exposure dose of 180mJ cm^{-2}.

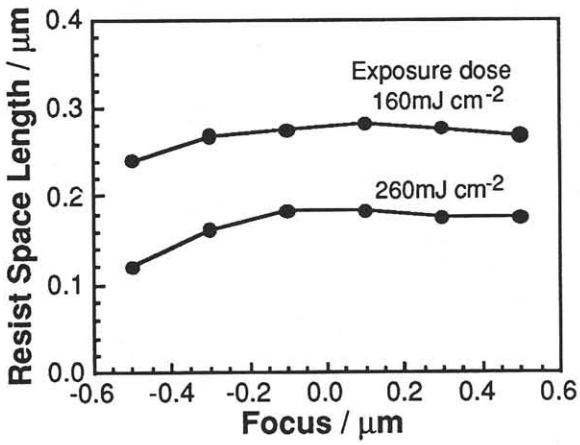

Fig.3 Relation between space length of LMR-UV and focus variation.

of 0.15-0.35μm by the exposure dose. The relation between space length and focus variation is shown in Figure 3. The focus margin of more than 1μm is obtained for 0.18μm space pattern.

3. Application to the Gate Pattern of Microwave GaAs Devices

In the PEL mask method, a closed loop pattern is formed on the resist corresponding to the phase-shifter edge. In order to form real gate pattern on the LMR-UV, we devised double exposure process. Figure 4 shows the PEL mask (a), which consist of phase-shifter for gate and opaque pattern of chrome for contact pad, and the developed resist pattern (b). To eliminate the unnecessary shifter edge pattern, 2nd exposure was done using additional mask (c) after the exposure with mask (a). The developed resist pattern was shown in (d). A gate pattern and a contact pad were formed simultaneously without change of pattern length at the connected point between them.

The closed circles in Figure 2 show the relation

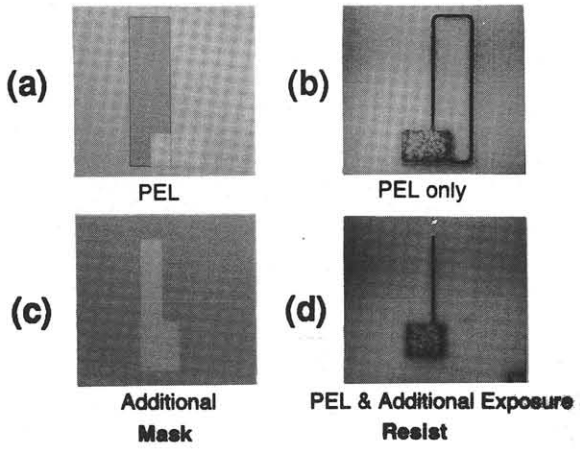

Fig.4 Photograph of mask and resist pattern. (a) PEL mask with opaque pattern, (b) resist pattern by using mask(a), (c) additional mask, (d) resist pattern using mask(a) and (c).

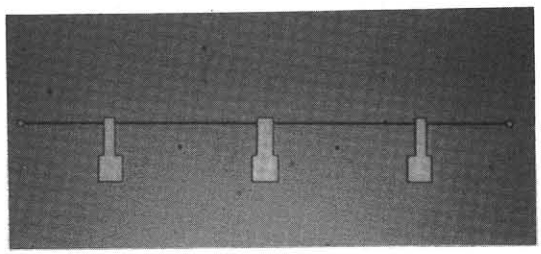

Fig.5 Resist pattern of 150μm-wide gate with three contact pads for microwave GaAs devices.

between space length for gate and the 2nd exposure dose at the constant 1st exposure dose. The resist space length was not influenced by the 2nd exposure with additional mask. Figure 5 shows the resist pattern of 150μm-wide gate for microwave GaAs devices. Multiple contact pads were formed simultaneously.

4. Fabrication Process of Microwave GaAs Devices

This technique was applied to the gate formation process of conventional AlGaAs/GaAs HEMTs[5]. The process flow is as follows. 1) Gate pattern was defined on LMR-UV coated on top of a SiN-deposited HEMT substrate. 2) SiN film was etched by reactive ion etching, 3) the HEMT substrate was recessed by wet etching using SiN film as a mask. 4) Gate metal (Al/Ti) was evaporated with tilted angle of 10° from vertical direction to the substrate and lifted off. Figure 6 shows the cross section of 0.18μm gate deposited on the recessed region.

The parameters related to the electrical characteristics are the gate length and the length of recessed region. These parameters are determined by the space length of the top of resist, its thickness and overhung profile. Because the PEL mask method has high resolution and wide focus latitude, the range of resist thickness in which fine line can be resolved is as

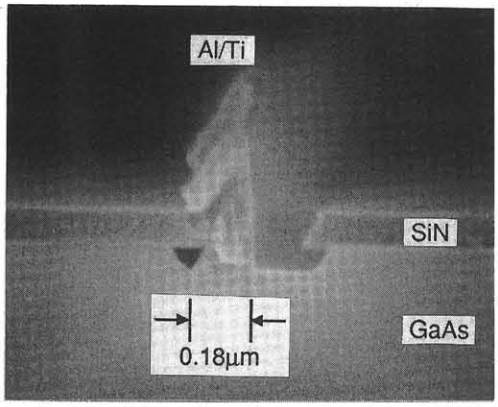

Fig.6 Cross sectional SEM photograph of 0.18μm gate formed by evaporation and lift-off process.

large as 1.0μm. Therefore, this method has wide process margin for dry etching process and for evaporation and lift-off process.

5. Electrical Characteristics of HEMTs

DC characteristics of 0.18μm gate HEMTs (W_g=10μm) are listed in Table 1 with the space length of resist for gate in a 3-inch wafer. The standard deviation of threshold voltage ($\sigma_{V_{th}}$) was 81mV and that of maximum transconductance (σ_{g_m}/g_m) was 2.2%. The good uniformity of transconductance was due to the small standard deviation of source resistance (σ_{Rs}/Rs) of 5.6%.

The cut off frequency ($f_T=v_s/2\pi L_g$) is a good measure of gate length. f_T at V_{ds}=2V, I_{ds}=15mA was in the range between 43.2 and 45.7GHz. The value of (max-min)/(2·mean)=2.7% of f_T was corresponded well to the standard deviation of resist space length for gate as shown in Table 1. The noise performances of the 150μm wide HEMTs with three feeds airbridge are shown in Figure 7. The minimum noise figure (F_{min}) at 12GHz was in the range of 0.56-0.58dB and the associated gain (G_{as}) was in the range of 10.9-11.1dB.

These very uniform DC and microwave characteristics are due to the uniformity of gate length and the profile of recessed region. These parameters can be controlled by the exposure dose using the gate PEL mask with respect to the device specification.

6. Conclusion

The PEL mask method using i-line stepper was applied to the gate formation process of AlGaAs/GaAs HEMTs. The double exposure process was developed to form real gate pattern and contact pad. The DC and microwave performances of these devices are excellent and very uniform. These results are due to the uniform distribution of gate resist pattern and the resist profile with high aspect ratio. The PEL mask method with high resolution and wide focus margin has the great advantages for microwave GaAs devices and also for ultra high speed GaAs LSIs.

Resist space length / mean / std. dev.	0.178μm 0.007μm
Vth / mean (Wg=10μm) / std. dev.	-0.34V 0.081V
gmmax (Wg=10μm) / std. dev.	407mS/mm 9mS/mm
fT (Vds=2V, Ids=15mA)	43.2-45.7GHz
Fmin (12GHz, Wg=150μm)	0.56-0.58dB
Gas (12GHz, Wg=150μm)	10.9-11.1dB

Table 1 Space length of resist for gate and electrical characteristics of 0.18μm gate HEMTs in a 3-inch wafer.

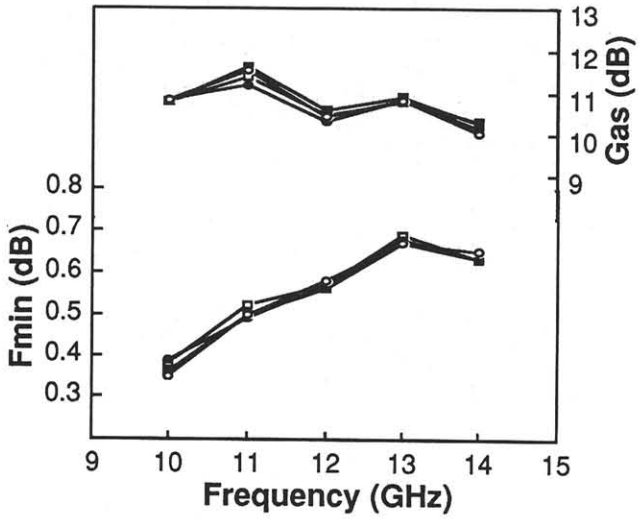

Fig.7 Frequency dependence of minimum noise figure (F_{min}) and associated gain (G_{as}) of 0.18μm gate HEMTs in a 3-inch wafer.

Acknowledgements

The authors are grateful to Dr. H. Nakamura, M. Kasashima and S. Kuribayshi for designing mask and measurement of Microwave characteristics.

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